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Optimization of Short-Channel RF CMOS Low Noise Amplifiers by Geometric Programming

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OPTIMIZATION OF SHORT-CHANNEL RF CMOS LOW NOISE AMPLIFIERS BY GEOMETRIC PROGRAMMING

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Abstract

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Geometric programming (GP) is an optimization method to produce globally optimal circuit parameters with high computational efficiency. Such a method has been applied to short-channel (90 nm and 180 nm) CMOS Low Noise Amplifiers (LNAs) with common-source inductive degeneration to obtain optimal design parameters by minimizing the noise figure. An extensive survey of analytical models and experimental results reported in the literature was carried out to quantify the issue of excessive thermal noise for short-channel MOSFETs. Geometric programming compatible functions have been determined to calculate the noise figure of short-channel CMOS devices by taking into consideration channel-length modulation and velocity saturation effects.

Optimal design parameters (e.g., channel width and noise figure) from geometric programming optimization are validated by comparing them with numerical simulations using Agilent's Advanced Design Systems (ADS) software. Furthermore, tradeoff analyses have been performed to examine the influence of various design parameters such as quality factors and drain current on the optimization of CMOS LNAs. In particular, it is found that the optimal input quality factor is slightly higher for LNAs using short-channel devices compared with the analysis reported for long-channel designs. With the continuous downscaling of CMOS technologies nowadays, geometric programming offers high performance advantages in the optimal design of short-channel CMOS LNAs.

Chapter One
Introduction

Radio frequency (RF) devices receive and transmit signals from 3 kHz to 300 GHz, covering a variety of wireless applications [1]. For example, broadcasting at radio frequencies has been established on technique for almost a century. Cellular phones have been used for decades. New generations of cellular phones (4G) have just been available for a couple of years. Moreover, wireless local area network (Wi-Fi) is gaining popularity for laptop, tablet and smartphone users, since Wi-Fi can provide access to the Internet via an access point (hotspot). Campus-wide Wi-Fi and city-wide Wi-Fi are further providing convenience for these users. Other applications of RF include global positioning system (GPS), phased array RF systems, radio frequency identification devices (RFIDs) and smart handheld devices [2]. Since wireless communication enables voice, data, image and video to be transferred to anywhere almost instantaneously, the impact of RF on people's daily lives has become significant.

The design of RF applications involves an important component known as the low-noise amplifier (LNA). The LNA is an essential component located at the first stage of a radio receiver circuit. The major function of an LNA is to amplify very weak signals (e.g., electrical signals received by an antenna) while adding as little noise and distortion as possible [3]. This is particularly true for applications in wireless and mobile communications with high frequency receivers. The optimization of low-noise amplifiers will minimize noise under power constraints, which is extremely important for mobile communications.

1.1 RF CMOS

Since there is a wide range of applications for RF, the implementation of LNAs depends on the specifics of each application. Historically, bipolar transistors have been

used for the design of high-power amplifiers in audio equipment and radio receivers [4]. Recently, submicron CMOS has become viable for the implementation of LNAs in wireless communication (e.g., cellular phones, Wi-Fi) due to its high integration feature and improvements in unity-gain frequency (ω_T) of MOS devices [5]. Four commonly used topologies are briefly described to satisfy the design requirements of low-noise amplifiers.

1.1.1 Bipolar vs. CMOS for RF Circuits

Classic devices in RF receivers consist of bipolar transistors and CMOS. For RF receiver applications, an optimal solution can be achieved by taking considerations of gain, noise, linearity, power consumption and cost.

One of the semiconductor devices commonly used for amplification is a bipolar transistor. Two major types of bipolar transistors are PNP and NPN. Bipolar transistors have pros and cons compared with CMOS. Bipolar devices can switch signals at high speeds, and can be manufactured to handle large currents so that they can serve as high-power amplifiers in audio equipment and in radio receivers. However, bipolar devices are not especially effective for low power design and are not suitable for high-integration applications, especially when integration with CMOS digital circuits is required.

The advantages of CMOS implementations for RF circuits are high integration density, low cost and exceptional speed performance when the devices are implemented in nanoscale technologies [2]. With the increasing popularity of system-on-chip (SoC) designs for increasing integration density and reducing system cost, CMOS implementations are very attractive for the realization of mixed-signal and RF designs [6]. Significant improvements for transit time and maximum oscillation frequency have been achieved when the CMOS gate length is scaled below 100 nm [7]. CMOS technology remains the major player for the market of low cost and less performance-demanding applications such as GPS, Bluetooth and Wi-Fi [2].

The shortcomings of CMOS in RF circuits are that the noise/gain performance and breakdown voltage of MOSFETs are not as good as that of bipolar devices. Nevertheless, such limitations can be overcome with appropriate circuit architectures.

Consequently, CMOS RF circuits have been used in 3G and 4G cellular applications, such as GSM/GPRS/EDGE [8].

1.1.2 RF CMOS LNA Topologies

The design of RF CMOS low-noise amplifiers typically involves a critical requirement to provide a specific impedance (i.e., 50 Ω) to the input source. Several topologies are available [3], including resistive termination, shunt-series feedback, $1/g_m$ termination, and inductive degeneration.

In resistive termination topology, a 50 Ω resistor (R) is simply placed across the input terminals of a common-source amplifier (Figure 1.1) with a source resistance R_s and an output resistance R_L. However, this additional resistor introduces thermal noise and attenuates the signal before the transistor, resulting in unacceptably high noise.

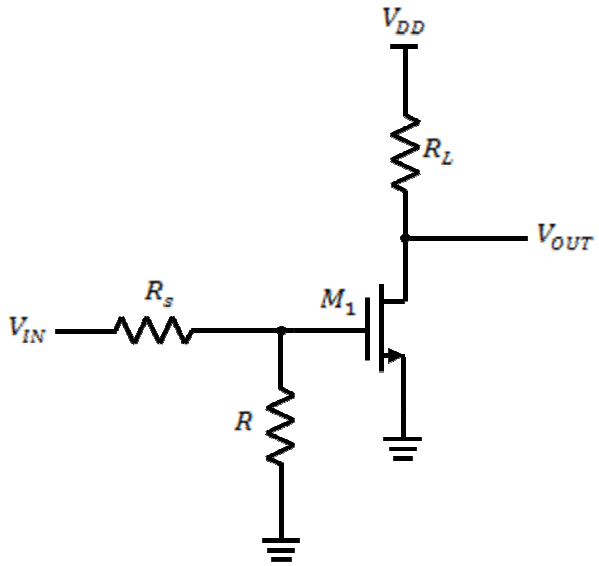


Figure 1.1: Common-source amplifier with resistive termination

In a shunt-series feedback topology (Figure 1.2), the resistor R does not cause attenuation of signals before amplification. It is expected that the noise figure in a shunt-series feedback amplifier is an improvement over that of a resistive termination amplifier. On the other hand, the resistor feedback network remains a source of thermal noise. Consequently, the noise performance of this topology is still not optimum.

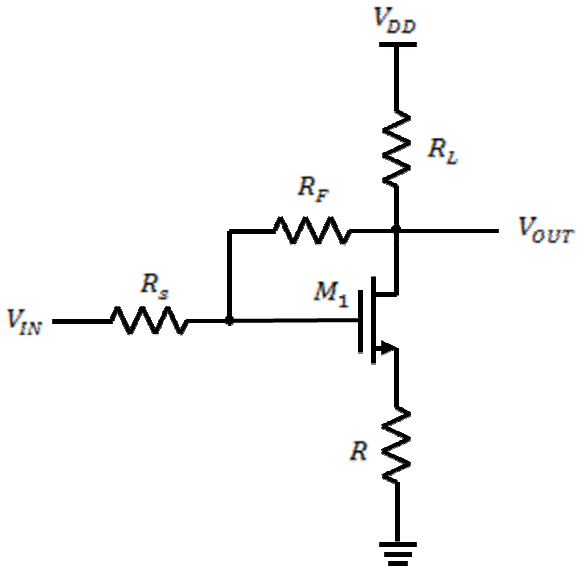


Figure 1.2: Shunt-series feedback amplifier

The common-gate topology ($1/g_m$) is another circuit implementing a resistive input impedance (Figure 1.3). One of characteristics of the common-gate topology is that the resistance looking into the source terminal equals $1/g_m$.

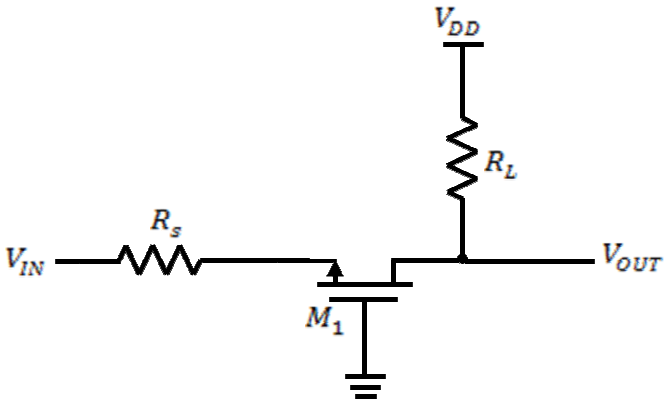


Figure 1.3: Common-gate amplifier

The aforementioned topologies do not have attractive noise performance due to the presence of a noisy resistance along the signal path. If a resistive input impedance can be provided without using an actual resistor, the noise performance of amplifiers can be significantly improved.

To create a resistive input impedance without the noise of real resistors, an inductive source degeneration topology (Figure 1.4) is commonly used. The key point of

this topology is that the input impedance has a resistive component. Conceptually this happens because a phase lag occurs at the potential of the bottom plate of the gate, which varies along the channel and depends on the signal at the gate. The additions of the source inductor L_s and the gate inductor L_g enhance this effect and provide control over the value of the input impedance [3]. Therefore, this topology provides a resistive input impedance at the resonant frequency without the thermal noise of an ordinary resistor and degrading the noise performance of the amplifier.

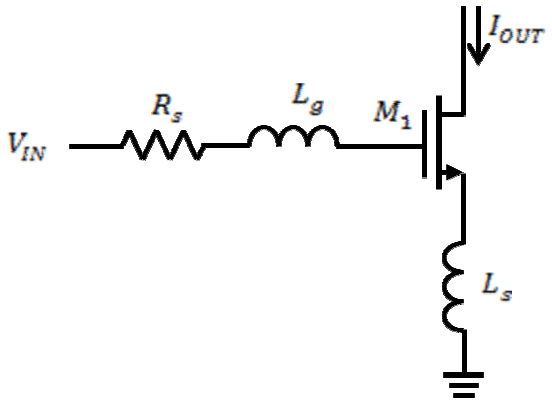


Figure 1.4: Narrowband LNA with inductive source degeneration

1.2 Submicron CMOS Technology

In the past three decades, the downscaling of CMOS technologies has continued to change the speed, complexity, and power consumption of many applications [9]. The introduction of submicron CMOS technology has posed new challenges to the design of analog circuits such as RF low-noise amplifiers due to various submicron effects [6].

1.2.1 Submicron Effects

The evolution of CMOS from the micron level to the submicron level contributes to new challenges in the design of analog circuits [10]. The first concern with downscaling of CMOS technology is the reduction in power supply voltage. Another problem is short-channel effects, such as velocity saturation and channel-length modulation, which have posed more difficulties for the modeling of short-channel MOSFETs.

Decreases in power supply voltage may result in lower performance of analog circuits. The drop of power supply voltages from 5 V to 1.2 V in submicron CMOS

technology may not pose serious problems in the design of analog circuits. However, further reduction of power supply voltages may cause technical challenges. For example, the reduction of power supply voltages results in analog circuits with lower performance since biasing at lower voltages causes the degradation of transistor properties [10]. Another problem with the reduction of power supply voltages is the loss of headroom required to employ cascoded load devices for high-gain amplifiers. This can cause a significant reduction in the output swing of the CMOS amplifier resulting in an amplifier with degraded performance [10].

When device geometries shrink down to the submicron level and beyond, various second order effects become prominent [3]. The velocity saturation of the carriers in the channel is a prime concern. Velocity saturation occurs when the electric field in the channel reaches a critical value which causes the carrier velocities to reach a maximum value. This means the drain current saturates sooner for short-channel devices when compared with long-channel devices. Channel-length modulation is another concern. For long-channel devices, a constant saturation drain current is assumed. However, this is not the case for short-channel devices. The extent of the depletion region close to the drain increases with the increasing drain to source voltage [3]. Drain current increases with the increasing drain to source voltage, which causes a nonzero output conductance. Thus, the modeling of MOSFETs needs to be reconsidered for short-channel devices.

1.2.2 Effect of CMOS Downscaling on Noise Model Analysis

The continuous downscaling of CMOS technologies requires that accurate modeling of noise be established when applied to the design of RF CMOS low-noise amplifiers. Thermal noise is the dominant source of noise for CMOS circuits at RF frequencies. The classical theory of thermal noise is still valid at the submicron level if short-channel effects are properly taken into account. Velocity saturation, channel-length modulation and hot carrier effects need special attention for submicron CMOS technologies.

The effect of velocity saturation on the noise performance of CMOS transistors becomes noticeable when the size of CMOS device scales down to the submicron level. Due to scattering by high-energy phonons, carrier velocities saturate and stop increasing

with increasing electrical field. The electron drift velocity finally saturates at a value of about 10^5 m/s when the electrical field reaches about 10^6 V/m in CMOS devices [3]. The drain current for calculating long-channel devices can be modified to reflect the effect of velocity saturation in short-channel devices. Details of such modification are available in the literature [11]. The drain current of short-channel devices becomes saturated and has a linear relationship, rather than a square-law relationship, with the gate-source voltage. Thus, thermal noise due to the drain current can be appropriately revised for short-channel devices by taking into consideration the effects of velocity saturation.

1.3 Optimization in Design of RF CMOS LNA

Wireless and mobile communication systems today are very complex and the time to market requirements create a short turnaround time, especially in today's competitive marketplace. Simulation becomes a critical tool to discover and correct problems before fabrication. Without such a tool, refabrication of an integrated circuit (IC) due to design miscalculations is very expensive and time consuming. Optimization techniques are a central component for the simulation tool to find the optimum design parameters to achieve the best performance. The optimization of CMOS LNA designs focuses on minimizing the noise figure in CMOS devices for a set of specifics, such as power dissipation, and transistor dimensions.

1.3.1 Optimization Methods

The design parameters in LNAs consist of transistor dimensions (e.g., transistor gate length L and gate width W) and other passive component values such as inductance and capacitance. The objective of optimization methods for low-noise amplifiers is to minimize the noise figure while optimizing other performance parameters. Various approaches are available for achieve this design optimization.

General-purpose classical optimization methods are extensively used in the computer aided design of analog circuits [12]. These classical methods include steepest descent, sequential quadratic programming, and Lagrange multiplier methods. The advantage of these classical methods is the ability to handle a large variety of problems. The disadvantage of these classical methods is that only a locally optimal design is found. The locally optimal design does not guarantee the design is the best design available

globally. As an analogy, someone walking in the mountains may see only the nearest peak, not the highest peak in the mountain range.

Another approach for design optimization is based on knowledge and expert systems [12]. The advantage is that it can be used anywhere with even fewer limitations than the classical optimization methods. The disadvantages of this approach include a locally optimum design, no detection of feasibility, and substantial human intervention.

Global optimization methods have the ability to find the globally optimal design and have been widely used in the computer aided design of analog circuits [13]. Two well-known methods of global optimization are branch and bound and simulated annealing. The advantages of global optimization methods are unambiguously achieving a global optimum and handling a wide variety of performance measures and objectives. The disadvantage is that global optimization methods can be very slow.

Convex optimization and geometric programming methods have started to gain attention in the computer aided design of analog circuits in recent years [13]. The advantages of convex optimization are efficiency of solving large problems with thousands of variables and tens of thousands of constraints, globally optimum solutions, and unambiguous detection of infeasibility. The disadvantage of convex optimization is that there are more limitations on the types of problems to be solved than the aforementioned methods for optimization. However, this is a compromise to achieve efficiency in solving large problems.

1.3.2 Geometric Programming

A geometric programming is an optimization problem of the form with the objective function as posynomial function and constraints of posynomial inequality and monomial equality. All design parameters are non-negative variables. A geometric programming problem can be converted to a convex optimization problem.

Geometric programming has been used in many problems in analog circuit and digital design [14]. For example, component values and transistor dimensions of CMOS operational amplifiers have been optimized by formulating geometric programming to meet the competing performance measures such as power, open-loop gain and bandwidth

[13]. Additional applications of geometric programming include RF circuit design [15, 16].

More importantly, geometric programming has recently been utilized for the design of RF CMOS low-noise amplifiers [17]. A low-noise amplifier with a topology of source inductive degeneration [18] using standard 0.35 μm CMOS process was optimized with the noise figure as the objective function and design constraints such as input circuit quality factor and input impedance matching. Globally optimum solutions were obtained with an extremely small computational cost.

This implementation of geometric programming focused on the intermediate channel length regime of the CMOS process. With the downscaling of CMOS technologies to submicron and nanoscale levels, the complexity of noise models for short channels poses challenges to formulate the objective function and design constraints in the form of geometric programming.

1.4 Objective of the Thesis

The objective of this thesis is to obtain the globally optimal design of RF CMOS low-noise amplifiers with short-channel devices by implementing geometric programming for minimizing the noise figure and for satisfying design constraints such as input circuit quality factor, power consumption, and input impedance matching.

A framework for noise modeling of short-channel RF CMOS transistors is first established by taking into consideration the velocity saturation effect. Then, the objective function of the noise figure is formulated in the form of a posynomial function and design constraints are described in the form of a posynomial inequality and monomial equality. After that, geometric programming is applied to obtain the globally-optimal solution. Design parameters from the optimal solution are compared with simulation results. Finally, the implication of geometric programming for short-channel CMOS designs is discussed and future work in this area is described.

Chapter Two
Noise Modeling in CMOS

In this chapter, major thermal noise models for MOSFETs in the literature are discussed, taking short-channel effects into consideration, such as velocity saturation, channel-length modulation, and the effect of mobility degradation. Most of these noise models are good for short-channel devices. A noise model suitable for geometric programming has been chosen for this study.

2.1 RF Noise

In general, noise means any unwanted signal. It is the opposite phrase to signal in electronics. Therefore, it can be defined as "everything except the desired signal" [3]. There are noise sources called artificial noise that can be reduced or removed using a good shielding system. An example is the interference between two adjacent cables transmitting voice or data information. On the other hand, noise sources that are inherent and irreducible in the system or devices are known as fundamental noise, for example, the snowy pictures in analog TV sets. The mystery of fundamental noise was unfolded by a series of papers written by H. Nyquist, J.B. Johnson and W. Schottky [19-21] with explanations of the origins of different noise sources and numerous analyses. In general, there are several types of fundamental noise sources: thermal noise, shot noise, flicker noise, and generation-recombination noise.

In MOSFETs, thermal noise and shot noise are the major noise sources. Flicker noise is known for its 1/f characteristic, which suggests that the power spectral density of flicker noise increases as frequency decreases. Therefore, flicker noise is insignificant in RF noise modeling but it is dominant at the low frequency range. Generation-recombination noise can be generally neglected since it is even much smaller than flicker noise. In RF MOSFET transistors, shot noise plays the main role in the noise characteristics only when the device is in the subthreshold region [3]. For low-noise

amplifier design, transistors are operating in the saturation region where shot noise can be neglected. Therefore, thermal noise is the focus for the noise analysis in this thesis.

2.2 Thermal Noise

Thermal noise, also known as Johnson-Nyquist noise, can be considered as a phenomenon of Brownian motion [21]. Thermally-excited carriers (usually electrons) generate a randomly varying current in a conductor. Because of the randomness of the noise process, it is impossible and meaningless to identify an exact value for the noise voltage at a particular time. In order to characterize the thermal noise, statistical measures are commonly used in noise analysis. Due to the thermal origin, the noise mean square value of a conductor is dependent on the absolute temperature [19]. Therefore, the thermal noise mean square value for a resistor is determined only by the temperature T and electrical resistance R at thermal equilibrium [3]:

$$\overline{e_n^2} = S_{e_n}\Delta f = 4kTR\Delta f \tag{2.1}$$

$$\overline{i_n^2} = \frac{\overline{e_n^2}}{R^2} = \frac{4kTR\Delta f}{R^2} = \frac{4kT\Delta f}{R} = S_{i_n}\Delta f \tag{2.2}$$

where S_{e_n} and S_{i_n} are the spectral densities of $\overline{e_n^2}$ and $\overline{i_n^2}$ for 1 Ω resistor respectively, k is Boltzmann's constant (1.38×10^{-23} V·C/K), Δf is the noise bandwidth in Hertz, and T is the absolute temperature in Kelvin. Thermal noise is also called white noise, because its mean square value is independent of frequency [22], as it is shown in aforementioned formulas. The two noise models for a resistor are depicted in Figure 2.1.

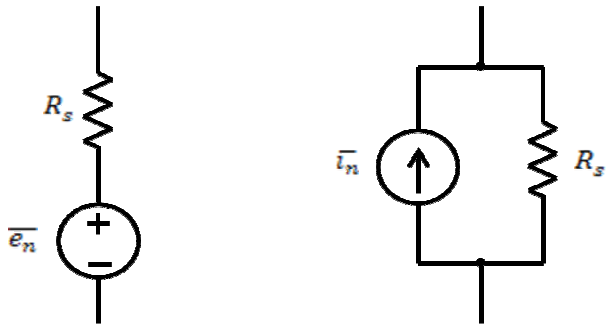


Figure 2.1: Thermal noise models for resistors [3]

The polarity signs for the noise voltage source and the noise current source do not indicate the noise has a particular polarity because noise has a zero mean voltage. They are simply references.

2.2.1 Thermal Noise in MOSFETs

MOSFETs behave basically as voltage-controlled resistors. Therefore, thermal noise is present in MOSFETs, which is the result of random potential fluctuations in the channel [23]. These fluctuations in the channel lead to one source of thermal noise, which is the drain current noise. In addition, through the oxide capacitance of the gate terminal, the fluctuations are introduced to the gate and cause a gate noise current, also known as induced gate thermal noise. The drain current noise and the gate noise are correlated because they both are agitated by the thermal noise sources in the channel. Since noise characteristics are one of the main concerns in the LNA design, it is very important for circuit designers to be able to predict and calculate the noise of MOS devices with reasonable accuracy and also to recognize the noise dependence on the geometry and biasing conditions of the device. Modeling of the thermal noise generated in the channel of MOSFETs started a few decades ago and much research on the compact modeling of thermal noise has been done [24].

2.2.2 Analytical Compact Thermal Noise Models

The fundamental assumption for most analytical and semi analytical MOSFET thermal noise models is the so-called gradual channel approximation (GCA). For the ideal two-terminal MOS device, the charge density profile is defined by a one-dimensional Poisson's equation, as it is described in the structure of a MOS capacitor. As for three-terminal or four-terminal MOSFET devices, they generally pose a two-dimensional electrostatic problem due to the geometric effects and the drain-source bias [25]. This approximation states that the rate of variation of the lateral field within the channel ($dE_{\parallel}/dx$) is much smaller than the rate of variation of the vertical field ($dE_{\perp}/dy$), as illustrated in Figure 2.2, and the channel potential is a gradually changing function of position along the channel from the drain to the source, which varies very little along the channel over a distance of the order of the gate oxide insulator thickness [11, 25, 26].

The GCA is valid for long-channel MOSFETs, where the aspect ratio between the gate length and the vertical distance of the space charge region from the gate electrode is large. Unfortunately, if the MOSFET is biased in strong inversion, which is in the saturation region, the GCA always becomes invalid beyond the pinch-off region due to the large lateral field gradient that develops in this region [22, 25]. Under the assumption of the GCA, a couple of noise models have been developed for long-channel MOSFETs.

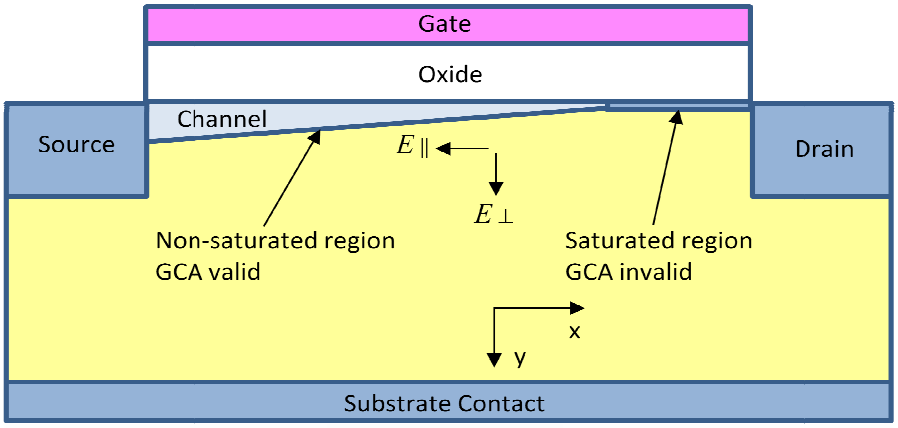


Figure 2.2: Gradual channel approximation [25]

2.2.2.1 The Model of Klaassen-Prins

Klaassen and Prins [27] were among the first researchers to develop equations for calculating the power spectral density of the thermal noise of a MOSFET. Their work is based on the relationship between the channel current and the local channel conductivity of the MOSFET. It has been widely used to calculate the channel thermal noise for long-channel MOSFETs [3, 22, 23]. The drain current of a MOSFET can be expressed in the following equation [23, 27] as

$$I_d = g\big(V(x)\big) \cdot \frac{dV(x)}{dx} \tag{2.3}$$

where $V(x)$ is the channel potential at x, $dV(x)$ is the dc voltage difference in the electron quasi-Fermi level in the inversion layer and the hole quasi-Fermi level in the substrate at position x (e.g. n-channel), and g is the local channel conductivity. A schematic representation is shown in Figure 2.3. For a simple long-channel MOSFET using the gradual channel approximation [23], the following can be written,

$$g\big(V(x)\big) = \mu C_{ox} W\big(V_{od} - V(x)\big) \tag{2.4}$$

where V_{od} is the overdrive voltage and it equals $V_{gs} - V_{th}$ (V_{gs} is the gate-source voltage, V_{th} is the threshold voltage), $V(x)$ is the channel potential at x, W is the width of the MOSFET, μ is the mobility, and C_{ox} is the oxide capacitance per unit area. Assuming a differential segment Δx of the channel, a small noise voltage contribution $v(x)$ across the segment Δx is observed, which is added to the dc voltage $V(x)$. This voltage can cause noise in the drain current, which leads to a change in the dc current through the MOSFET. There are some assumptions throughout the following analysis. First, noise sources of the different channel segments are local and not correlated. Second, the charge carriers are in thermal equilibrium. The boundary conditions of the small voltage contribution $v(x)$ are $v(x)|_{x=0,L} = 0$ [23, 27]. Therefore, the Klaassen-Prins equation for the power spectral density S_{i_d} of thermal noise of a long-channel MOSFET is

$$S_{i_d} = \frac{4kT}{L^2 I_d} \int_0^{V_{ds}} g^2(V) \cdot dV \tag{2.5}$$

where I_d is the drain current, L is the gate length and $g(V)$ is the local output conductivity. This equation can be developed into another commonly used expression, which is the so-called white noise gamma factor formula discussed in the following section. The details for this derivation can be found in Appendix A.

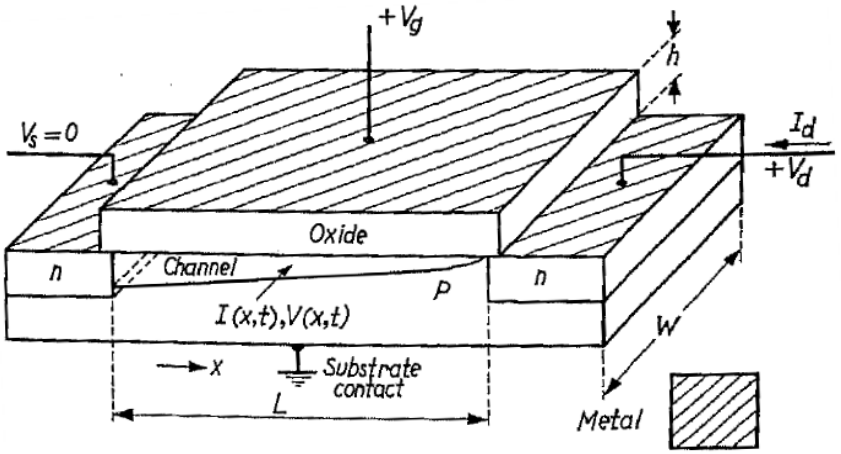


Figure 2.3: Schematic representation of an n-channel MOSFET transistor [27]

2.2.2.2 The Model of Albert van der Ziel

After Klaassen and Prins introduced their model for channel thermal noise in MOSFETs, Albert van der Ziel included hot electron effects in his model by substituting the lattice temperature with carrier temperature, $T_e(x)$, and modified the model to [23]

$$S_{i_d} = \frac{4kT}{L^2 I_d} \int_0^{V_{ds}} \frac{T_e(x)}{T}\, g^2(V) \cdot dV \tag{2.6}$$

Once $\frac{T_e(x)}{T}$ and $g(V)$ are known, S_{i_d} can be easily calculated. In order to treat a MOSFET as resistor element, van der Ziel presented a convenient expression [23]:

$$S_{i_d} = 4kT\gamma g_{d0} \tag{2.7}$$

where

$$\gamma = \frac{1}{g_0 I_d L} \int_0^{V_{ds}} \frac{T_e(x)}{T}\, g^2(V) \cdot dV \tag{2.8}$$

In Eq. (2.8), g_0 is the channel conductance per unit length at the source and $g_{d0}$is the channel conductance at zero drain bias. The parameter γ is often called the white noise gamma factor and the expression in Eq. (2.8) is commonly used to calculate and demonstrate the channel thermal noise in long-channel MOSFETs and the excess channel thermal noise in short-channel transistors. The parameter γ relates the thermal noise power spectral density with the output conductance at different bias conditions. However, it is very practical and continues to be used to allow experimental or theoretical results to be compared from different research groups [28]. The value of γ is unity for zero drain bias, in long-channel devices, and decreases toward 2/3 in saturation.

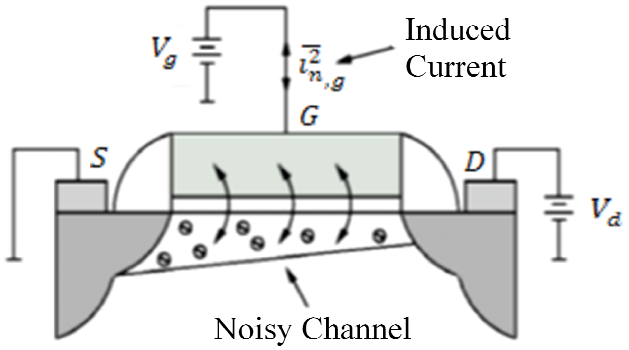
In addition, a MOSFET can be described as an RC network at high frequencies, with the oxide capacitance of the gate terminal and the resistance due to the channel itself. The fluctuations in the channel are introduced to the gate and cause a gate noise current, also known as induced gate thermal noise (Figure 2.4 (a)). Van der Ziel has shown the induced gate noise can be expressed as [23]

$$S_{i_g} = 4kT\beta g_g \tag{2.9}$$

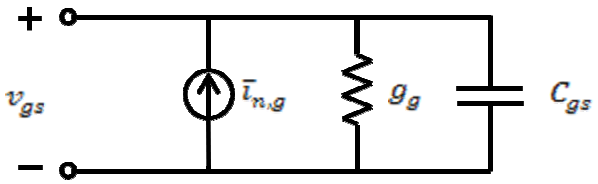
where β is basically independent of the substrate conductivity, and its value is 4/3 in the saturation region for long-channel MOSFETs. The conductance g_g has the form as

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{2.10}$$

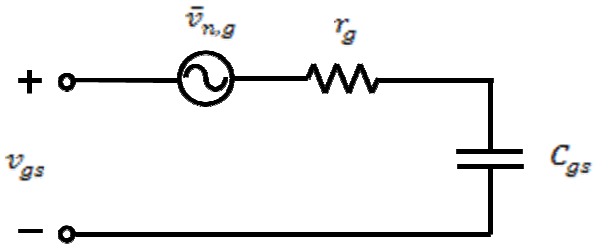
In Eq. (2.10), the intrinsic gate capacitance of transistor $C_{gs} = \frac{2}{3} C_{ox} WL$ where C_{ox} is the oxide capacitance per unit area, W is the channel width and L is the channel length. A circuit model for gate noise has been illustrated in [3], which describes the induced gate noise in the form of Eq. (2.9).



(a)



(b)



(c)

Figure 2.4: (a) Induced gate noise, (b) Standard representation, (c) Equivalent Thévenin representation [29]

In the circuit model representation, the conductance g_g is connected between the gate and source shunted by the gate noise current. An equivalent Thévenin representation seems more intuitive with $r_g = \frac{1}{5g_{d0}}$ [3]. As shown in Eq. (2.10), the conductance g_g increases with frequency, indicating that the induced gate noise can dominate at radio frequencies. The conductance g_g is also proportional to the square of C_{gs}, so a small value of C_{gs} will favor a lower induced gate noise. This is discussed further in the following chapter.

Since the induced gate noise is correlated with the drain thermal noise, the correlation coefficient is defined as [23]

$$c = \frac{\overline{\iota_{ng} \cdot \iota_{nd}^*}}{\sqrt{\overline{\iota_{ng}^2} \cdot \overline{\iota_{nd}^2}}} \tag{2.11}$$

where $\overline{\iota_{ng} \cdot \iota_{nd}^*}$ is the spectrum of the crosscorrelation of the drain thermal noise and the induced gate noise. The complex correlation coefficient c is theoretically 0.395j for long-channel MOSFETs (see Appendix B).

2.2.2.3 The Model of Tsividis

Another frequently used equation for the channel thermal noise proposed by Tsividis is given by [22]

$$S_{i_d} = 4kT \frac{\mu}{L^2} (-Q_{inv}) \tag{2.12}$$

where μ is the carrier mobility and Q_{inv} is the total inversion layer charge.

The aforementioned models are developed and valid for long-channel MOSFETs, where short-channel effects were not taken into account. The short-channel effects, such as velocity saturation, enhanced channel-length modulation and mobility degradation, are basically caused by the high longitudinal field due to the short gate length of the MOSFET. Meanwhile, the GCA assumption becomes invalid due to the velocity saturation for short-channel MOSFETs. Additionally, considerable increase in the drain current noise of short-channel MOSFETs has been observed and becomes significant

while MOSFETs geometries shrink down to the submicron level [11, 22, 24, 25, 30, 31]. Therefore, several models have been developed to explain this enhanced thermal noise present in short-channel MOSFETs.

2.2.2.4 The Model of Scholten et al.

In the Klaassen-Prins model shown in Eq. (2.5), L is the MOSFET gate length and g is the local channel conductivity. This model is suitable for long-channel MOSFETs. Unfortunately, for submicron channel lengths, short-channel effects become more significant. Scholten and his colleagues developed a nonquasi-static RF MOSFET model based on the concept of channel segmentation [22, 30]. This was implemented in the so-called MOS Model 11 [32], where every channel segment is taken into account.

An improved Klaassen-Prins model including the effect of channel-length modulation and the effect of velocity saturation is presented in [28, 30, 33]. The noise power spectral density is

$$S_{i_d} = \frac{4kT}{L_{elec}^2 I_d} \int_0^{V_{ds}} g_c^2(V) \cdot dV \tag{2.13}$$

where L_{elec} is the electrical channel length of the MOSFET, replacing the effective channel length L_{eff} in the original Klaassen-Prins expression. The parameter L_{elec} is defined as $L_{elec} = L_{eff} - \Delta L$ where ΔL is the length of the velocity saturated region. The parameter g_c is the revised conductivity taking velocity saturation into consideration. The noise contribution of the pinch-off region is assumed to be negligible due to insignificant dependence of channel thermal noise on the drain-to-source voltage beyond the saturation voltage [30].

2.2.2.5 The Model of Han et al.

In Han's approach [31, 34], the effect of velocity saturation and the effect of carrier heating are taken into account. In long-channel MOSFETs, the carrier mobility is considered independent of the bias conditions and is usually modeled as a constant. However, the carrier mobility in short-channel MOSFETs is degraded due to the high lateral electric field from drain to source [11] and is thus dependent on the bias conditions. The impedance field method [35] was used to recalculate the thermal noise

for short-channel MOSFETs. The drain current of a MOSFET with the effect of mobility degradation is given in [34] as

$$I_d = g_0(V)\frac{\left(\frac{dV}{dx}\right)}{1+\left(\frac{dV}{dx}\right)/E_C} \tag{2.14}$$

where the local channel conductance $g_0(V) = \mu_{eff} W C_{ox}(V_{od} - \alpha V)$. The parameter $E_C = 2v_{sat}/\mu_{eff}$ is the critical field at which velocity saturation occurs, v_{sat} is the saturation velocity of carriers, μ_{eff} is the effective mobility, C_{ox} is the gate oxide capacitance per unit area, V_{od} is the gate overdrive voltage ($V_{gs} - V_{th}$), V is the source-referenced channel potential at x, and α is a coefficient describing the bulk-charge effect. The bulk-charge effect is the variation of threshold voltage caused by non-uniform channel depletion and the dependence of the threshold voltage on the channel potential. The impact of the carriers in the velocity saturation region on the drain thermal noise current is ignored in this analysis. Applying a similar procedure and method as Scholten, the channel noise of the MOSFET takes the form of

$$S_{i_d} = \frac{4kT}{L_{elec}^2 I_d (1+\frac{V_{ds}}{L_{elec}E_C})^2}\int_0^{V_{ds}} g_0^2(V)(1+\frac{E}{E_C})\cdot dV \tag{2.15}$$

where the electrical channel length of the MOSFET is $L_{elec} = L_{eff} - \Delta L$.

In order to obtain a compact analytical equation, a closed-form expression is given [34] as

$$S_{i_d} \approx 4kT g_{d0}\frac{1-u+\frac{u^2}{3}}{1-\frac{u}{2}} \tag{2.16}$$

where g_{d0} is the drain conductance at $V_{ds} = 0$ V, $u = \alpha V_{ds}/V_{od}$ and α is the coefficient of the bulk charge effect. The parameter α has a typical value of 1.2 [36]. The parameter V_{od} is the gate overdrive voltage, which equals ($V_{gs} - V_{th}$).

2.2.2.6 The Model of Deen et al.

Based on Han's model, the longitudinal electric field (E) along the channel was examined by Deen's group [24]. They claimed that the longitudinal electric field (E) is a function of the position x along the channel instead of a constant along the channel, and is given by

$$E(x) = \frac{E_C V_d}{[(2V_{od} - V_d)^2 - 4\alpha E_C V_d x]^{\frac{1}{2}}} \tag{2.17}$$

where $V_d = I_d/(WC_{OX}v_{sat})$. The revised total channel charge can be obtained by integrating the drain current from 0 to L_{elec} with the expression of $E(x)$ in Eq. (2.17). The total drain-current noise power spectral density is then obtained,

$$S_{id} = 4kT\frac{4V_{od}^2 + V_d^2 + V_{od}V_d}{3V_{od}^2(V_{od} - V_d)}\ \alpha I_d \tag{2.18}$$

2.2.2.7 The Model of Jeon et al.

Jeon and his colleagues also have developed an analytical channel thermal noise model for deep-submicron MOSFETs with short-channel effects [37]. By following Tsividis' method [22], they derived an analytical noise model. In their analytical channel thermal noise model, short-channel effects, such as channel-length modulation, velocity saturation, and hot carrier effects, have been taken into account.

The ac conductance g_{ac} is a small-signal conductance with the consideration of velocity saturation. It was used to express the current noise source spectrum of a small segment Δx of channel length, and it is given as

$$\overline{\Delta i_n^2} = 4kT_c g_{ac}\Delta f \tag{2.19}$$

where T_c is the carrier effective temperature. The carrier temperature has shown a dependency on the electric field when a high electric field is present in short-channel MOSFETs. The relation of T_c and the electric field is given as

$$\frac{T_c}{T_0} = \left(1 + \frac{E}{E_c}\right)^n \tag{2.20}$$

where T_0 is the lattice temperature, and when $n = 0$ the carrier is in thermal equilibrium without carrier heating effect. The heating effect is considered for $n = 1$ or $n = 2$ [23].

This small noise source will be added on the top of the drain current I_{ds}, which already includes the velocity saturation effect in this model [37]. By integrating the new drain current over the channel, the total drain-current noise power spectral density for different values of n is given as

$$S_{id} = 4kT_0 \frac{4V_{od}^2 + 10V_0^2 + 7V_{od}V_0 + \frac{3}{2}\frac{V_0^3}{V_{od}-V_0 ln\frac{|2V_{od}-V_0|}{V_0}}}{3(V_{od} - V_0)(V_{od} + V_0)^2} mI_d$$

$$with\ n = 2 \qquad (2.21a)$$

$$S_{id} = 4kT_0 \frac{4V_{od}^2 + 4V_0^2 + 4V_{od}V_0}{3(V_{od} - V_0)(V_{od} + V_0)^2} mI_d$$

$$with\ n = 1 \qquad (2.21b)$$

$$S_{id} = 4kT_0 \frac{4V_{od}^2 + V_0^2 + V_{od}V_0}{3(V_{od} - V_0)(V_{od} + V_0)^2} mI_d$$

$$with\ n = 0 \qquad (2.21c)$$

where V_{od} is equal to $(V_{gs} - V_{th})$, and $V_0 = I_d/(WC_{OX}v_{sat})$, which is the same as V_d in Deen's model. The parameter m is body effect factor [11]. These models show great similarity with Han's model and Deen's model, and were validated with measurement results by Jeon's group.

2.2.2.8 White Noise Factor Formula

The aforementioned models all included some of the short-channel effects based on different perspectives of the researchers, such as the effect of velocity saturation, the effect of channel-length modulation, and the effect of mobility degradation. However, the expressions in Eq. (2.13) and Eq. (2.15) are not suitable for hand analysis. Particularly, they are not practical for use in geometric programming, which is the special optimization method adapted in this thesis. A simpler noise formula would be a better

choice. As mentioned in the discussion of van der Ziel's model, the channel thermal noise can be conveniently expressed using the so-called white noise gamma factor formula given in Eq. (2.7), where γ is the thermal noise factor. Since this expression is a simple closed-form equation, it has been widely used for noise analysis by circuit designers, and it is also used in this thesis. For long-channel MOSFETs, the theoretical values of γ are well known. It is equal to unity at zero drain bias and 2/3 in the saturation region. However, when the size of MOSFETs approaches the submicron and even smaller level, it is observed that the values of γ are not the same as in long-channel MOSFETs under the same bias conditions. There are some reports regarding the modeling of γ in short-channel MOSFETs [30, 34, 38]. Since excess thermal noise has been observed in short-channel MOSFETs, an increase of the value γ is expected for short-channel MOSFETs.

In the work of Scholten and his group [30], measurements and modeling had been carried out. Short-channel effects, such as effect of velocity saturation and effect of channel-length modulation, have been taken into account in their noise modeling, which has been described in the previous section. Based on their results, both the channel thermal noise constant γ and the induced gate current noise constant β are independent of the operating frequencies within moderate frequencies (for example, 10 GHz or less), and they are not very sensitive to bias conditions for high bias voltages. However, they do vary with the channel lengths, which agreed with the fact that larger thermal noise was present in short-channel MOSFETs than long-channel MOSFETs. The values of γ are expected to be larger than their theoretical long-channel values. Because of the same origin of channel thermal noise and induced gate noise, a similar trend of increase in β has been observed at short channel lengths.

Jeon and his group recently have also investigated and measured the white noise factor γ [38], which is an extension of their previous work. The channel thermal noise power spectral density can still be expressed as Eq. (2.7), the well-known white noise gamma factor formula. However, the white noise factor γ for short-channel MOSFETs takes the form of

$$\gamma = \frac{g_{ds}}{g_{d0}}\left(1 + \frac{\bar{E}}{E_C}\right) \tag{2.22}$$

where g_{ds} is the conductance of the channel, $\bar{E}$ is the average longitudinal electric field which is equal to V_{ds}/L_{elec} .The parameter E_C is the critical electric field, which is equal to $2v_{sat}/\mu_{eff}$. Based on the model of Eq. (2.22), γ is a function of the drain bias for different channel length. A comparison between Deen's analytical model of the channel thermal noise in Eq. (2.18), and the thermal noise calculation using the two γ models from Scholten's and Jeon's results have been made. As it is shown in Figure 2.5, their results are comparable with a similar trend regarding different channel lengths. Since Scholten and Jeon have completed a relatively in depth study of the noise parameters and there is relatively good agreement of their work with Deen's analytical model, the noise calculations in this thesis are carried out based upon the results of Scholten and Jeon.

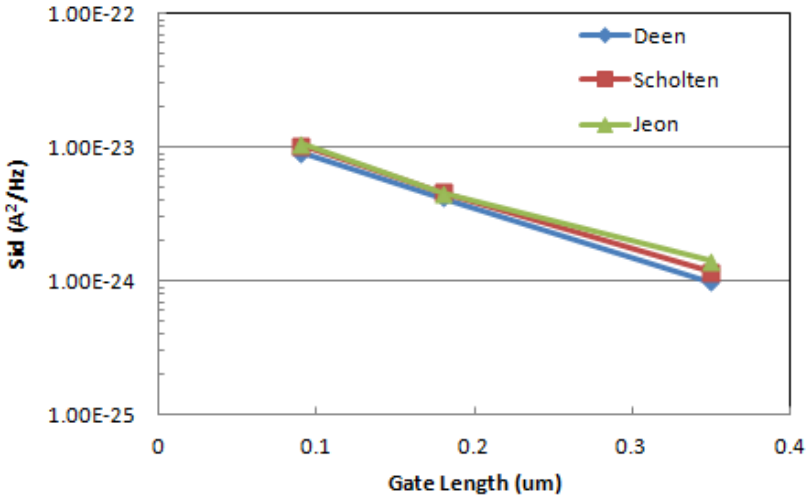


Figure 2.5: Thermal noise comparison of different analytical noise models

The numerical results for Figure 2.5 are shown in Table 2.1.

Table 2.1: Thermal noise comparison of different analytical noise models

Gate Length	Power spectral density of channel thermal noise (A^2/Hz)		
	Deen	Scholten	Jeon
90 nm	9.07×10^{-24}	1.04×10^{-23}	1.07×10^{-23}
180 nm	4.22×10^{-24}	4.63×10^{-24}	4.54×10^{-24}
350 nm	9.86×10^{-25}	1.17×10^{-24}	1.41×10^{-24}

2.3 Noise Parameters

Noise parameters are used to measure and evaluate the noise performance of a given system. The noise factor is a useful and important one among the noise parameters, which is usually denoted as F. If only the overall input-output behavior of a system is concerned, all the internal noise sources can be represented by a pair of external sources: a noise current and a noise voltage. The noise factor F is then defined as

$$F = \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source} \tag{2.23}$$

where the source temperature is at 290 K by convention [3]. The noise factor gives a quantitative evaluation of the degradation in the signal-to-noise ratio due to the system noise sources, which means the larger noise factor would be expected if the larger degradation in signal-to-noise occurs. Since the lower signal-to-noise ratio is always desired, the smaller noise factor is the optimum goal for LNA circuit designs. An alternative expression of the noise factor is the noise figure, which is commonly used and simply the noise factor expressed in decibels as

$$NF = 10\log_{10}(F) \tag{2.24}$$

In summary, different short-channel noise models have been reviewed and discussed in this chapter. The experimental results from Scholten's and Jeon's groups, which both take into account short-channel effects, have shown good agreement with Deen's analytical model. Therefore, an excess thermal noise model with elevated white noise gamma parameter following Scholten and Jeon has been chosen for the noise analysis in this study. In the next chapter, the derivation of the noise figure and the design considerations for low-noise amplifier optimization will be presented and discussed in detail.

Chapter Three

Formulation of Geometric Programming for Short-channel CMOS LNAs

Geometric programming is proposed as the method to optimize the design of short-channel CMOS LNAs. The objective function for geometric programming is to minimize the noise figure of the CMOS LNA subject to design constraints. The noise figure for short-channel devices is placed in the form of posynomial functions, which are compatible with geometric programming. In addition, design constraints, such as output conductance, transconductance, dimensional constraints, input impedance, and power dissipation are expressed either as a posynomial function or a monomial function.

3.1 Geometric Programming

A geometric optimization problem has an objective function in the form of a posynomial function with inequality constraints expressed as posynomial functions and equality constraints as monomial functions [14].

A monomial function has the following form:

$$g(x_i) = c\, x_1^{a_1} x_2^{a_2} x_3^{a_3} \dots x_n^{a_n} \tag{3.1}$$

where c is a positive constant ($c > 0$); x_1, x_2, …, and x_n are real positive variables; a_1, a_1, …, and a_1 are constants known as the exponents of the monomial. Any positive constant is a monomial. Monomials are closed under multiplication and division.

A posynomial function is a sum of one or more monomial functions as shown in the following equation,

$$f(x_i) = \sum_{k=1}^{K} c_k x_1^{a_{1k}} x_2^{a_{2k}} x_3^{a_{3k}} \dots x_n^{a_{nk}} \tag{3.2}$$

where $c_k > 0$. Note that posynomial functions are also closed under addition and multiplication.

With the introduction of the basic concepts for monomial and posynomial functions, a standard form for a geometric programming can be defined as an optimization problem with the following form

$$\begin{aligned} &\text{Minimize an objective function: } f_0(x) \\ &\text{Subject to constraints: } \quad f_i(x) \leq 1,\ i = 1, \cdots, m \\ &\qquad\qquad\qquad\qquad\quad g_i(x) = 1,\ i = 1, \cdots, p \end{aligned} \tag{3.3}$$

where $x = (x_1, \ldots, x_n)$ a vector with components x_i, $f_0(x)$ is an objective function with the form of a posynomial function; $f_1(x)$, $f_2(x)$, …, $f_m(x)$ are posynomial functions; $g_1(x)$, $g_2(x)$, …, $g_p(x)$ are monomial functions; and x_i are the optimization variables (x_i are always greater than zero).

As a global optimization method, geometric programming has provided a very efficient method for designing CMOS operational amplifiers [13] and RF CMOS low-noise amplifiers using long-channel MOSFETs [17]. In this thesis, geometric programming was applied to the design optimization of a short-channel CMOS narrowband low-noise amplifier. The frequency of operation was chosen to be 2.4 GHz, which is the operating frequency for widely-used Bluetooth applications. For narrowband operation, which is the focus of this thesis, inductive source degeneration offers the best noise performance compared to other topologies discussed previously in Chapter Two. Therefore, an LNA with inductive source degeneration, as shown in Figure 3.1, is selected for design optimization in this thesis. A cascode device M_2 is added to improve the isolation between the tuned input and tuned output circuits and also to reduce the effect of the gate-to-drain capacitance of transistor M_1 [3]. An additional capacitance C_e across the gate and source is introduced into the circuit, which is in parallel to the intrinsic gate capacitance C_{gs} of the transistor M_1. By adding this capacitor, a relatively high quality factor can be obtained without very high values of the on-chip inductors (L_g and L_s), which is very important for high-integration density circuit implementations.

This additional capacitance also gives the freedom to choose small intrinsic gate capacitance C_{gs}. Since the induced gate noise is proportional to the square of C_{gs}, smaller C_{gs} will result in a lower induced gate noise, which has been found to be more significant in short-channel devices [18]. The formulation of such a design problem as a geometric programming is shown in detail in this chapter.

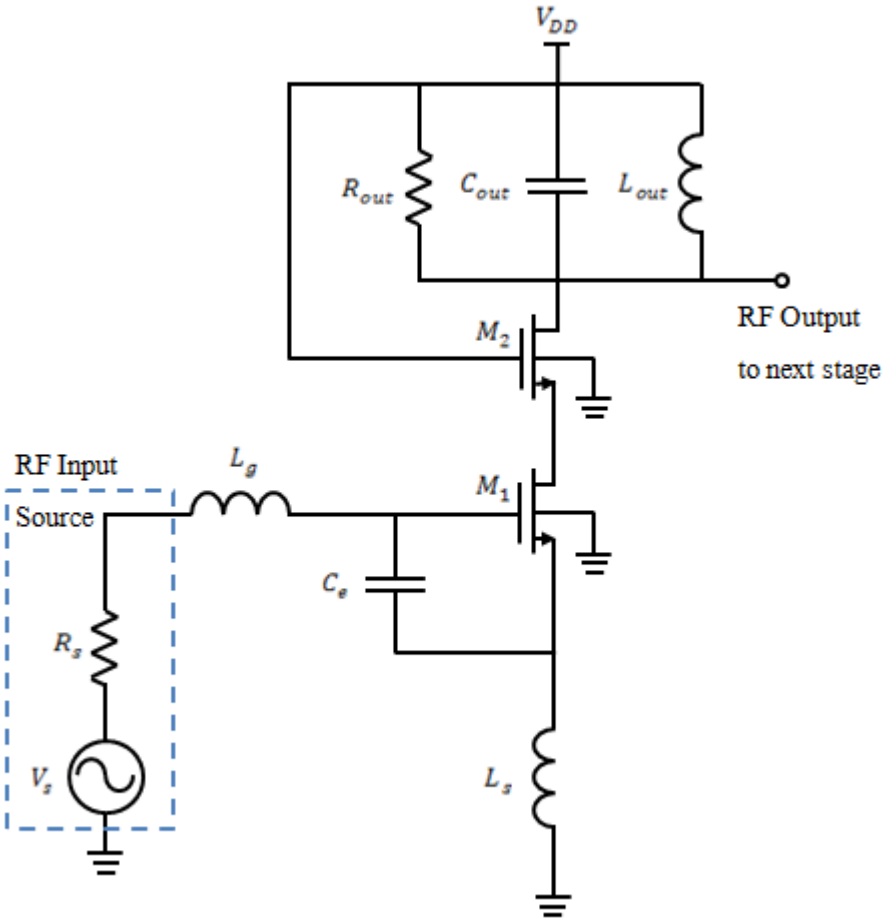


Figure 3.1: Schematic of CMOS cascode LNA with inductive source degeneration

3.2 Design Considerations for a Short-channel CMOS LNAs

The major goal of an LNA is to provide a reasonable gain with a small noise level. The noise performance is the most crucial issue for a front-end amplifier. Therefore, minimizing the noise figure is the main objective of the CMOS LNA design in this thesis. To achieve the best noise performance, design variables such as channel width (W) and channel length (L) need to be optimized. In addition, design constraints, such as

quality factor of the input circuit, maximum allowed power dissipation, and input impedance matching, need to be satisfied during the optimization process.

3.2.1 Objective Function

The objective of LNA design in this thesis is to minimize the noise figure. Consequently, the noise figure is considered as the objective function for geometric programming. By small-signal analysis, the equation for the noise figure is described in the following section.

Assuming the output impedance of transistor M_1 (r_{o1}) is large, transistor M_2 has an insignificant influence on the noise performance of the low-noise amplifier. Therefore, its contribution to the total noise is neglected in the noise analysis. In addition, the contribution of the substrate noise is also neglected as well for simplicity [18]. Therefore, the noise figure will be minimized for the given design constraints. Based on the previous discussion of noise sources in RF CMOS, the thermal noise is the main concern at RF intermediate frequencies (i.e., the carrier frequency) for MOSFETs, where 1/f noise is no longer significant. Therefore, four noise sources have been considered in the design, which are the thermal noise of the source resistance ($\bar{\imath}_{n,R_s}$), the channel thermal noise ($\bar{\imath}_{n,d}$), the gate induced current noise ($\bar{\imath}_{n,g}$), and the thermal noise of the output resistance ($\bar{\imath}_{n,R_{out}}$).

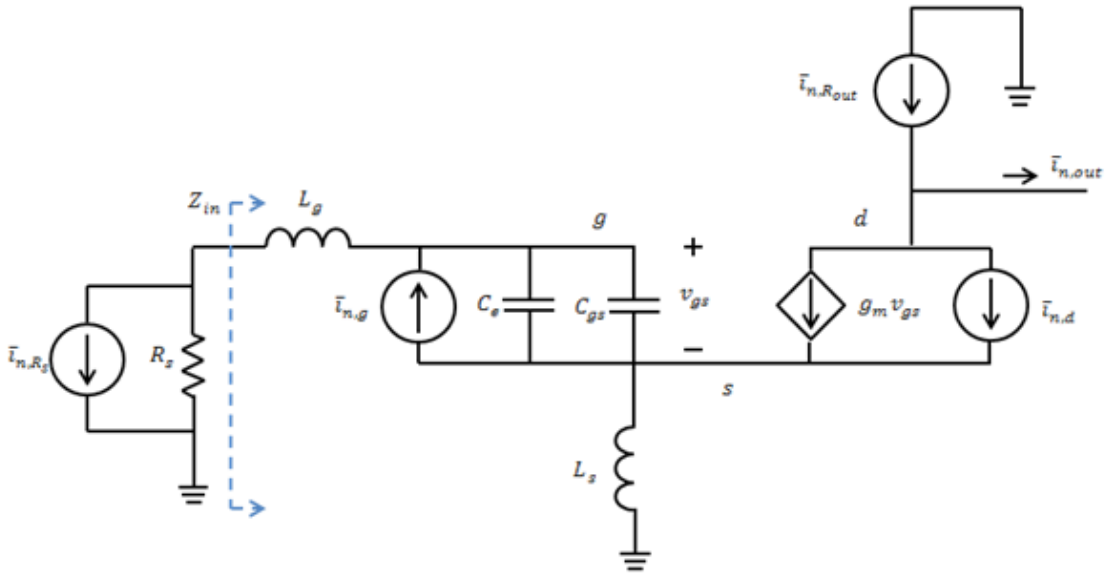


Figure 3.2: Small-signal circuit for noise analysis

Before the discussion of the noise analysis, the input impedance needs to be calculated in order to determine the noise contributions of the input referred noise in the following derivations. All the passive components in the circuit are considered to be lossless except the output load, which is represented by an LC tank including a parasitic resistance, as shown in Figure 3.1. To compute the input impedance of the circuit in Figure 3.2, the small-signal MOSFET is modeled only with a transconductance (g_m) and a gate-source capacitance (C_{gs}). The equivalent circuit to calculate the input impedance of the circuit is shown in Figure 3.3.

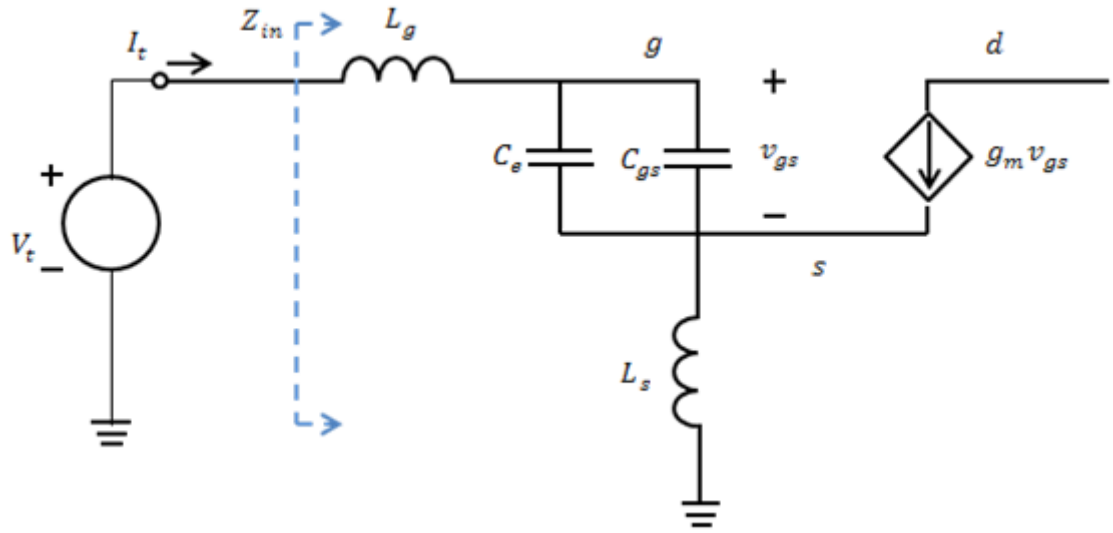


Figure 3.3: Equivalent circuit for the input impedance calculation

Therefore, the input impedance is (see Appendix C for the full derivation)

$$Z_{in} = \frac{V_t}{I_t}$$

$$= \frac{1}{j\omega(C_e + C_{gs})} + j\omega(L_g + L_s) + \frac{g_m}{(C_e + C_{gs})} L_s$$

$$= \frac{g_m}{(C_e + C_{gs})} L_s + j\left[\omega(L_g + L_s) - \frac{1}{\omega(C_e + C_{gs})}\right] \quad (3.4)$$

At the resonant frequency ω_0, which is the operating frequency of the circuit, the input impedance should be resistive and equal to the source resistance for the maximum

power delivery. In this case, the input resistance is R_s, which gives the following relation regarding the input impedance,

$$\omega_0(L_g + L_s) - \frac{1}{\omega_0(C_e + C_{gs})} = 0 \tag{3.5}$$

$$\frac{g_m}{(C_e + C_{gs})} L_s = R_s \tag{3.6}$$

After applying some simple algebra, the final equations required to obtain an input impedance match at the resonant frequency are

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)(C_e + C_{gs})}} = \frac{1}{\sqrt{L_{tot} \cdot C_{tot}}} \tag{3.7}$$

$$R_s = \frac{g_m}{(C_e + C_{gs})} L_s = \frac{g_m}{C_{tot}} L_s \tag{3.8}$$

where $L_{tot} = (L_g + L_s)$ and $C_{tot} = (C_e + C_{gs})$.

Since the focus is on the resonant behavior of the circuit, a commonly used parameter Q, which is called the quality factor, is introduced into the analysis. By definition,

$$Q = \omega \frac{energy\ stored}{average\ power\ dissipated} \tag{3.9}$$

The quality factor of a series RLC circuit is given as $Q = \frac{\sqrt{L/C}}{R}$ [3]. Therefore, the quality factor of the input circuit at resonant frequency ω_0 is described as

$$Q = \frac{\sqrt{L_{tot}/C_{tot}}}{R_{tot}} \tag{3.10}$$

where $R_{tot} = R_s + \frac{g_m}{C_{tot}} L_s$. Making use of Eq. (3.7) and Eq. (3.8), the quality factor of the input circuit at resonant frequency ω_0 has the form of

$$Q = \frac{1}{R_{tot}\omega_0 C_{tot}} = \frac{1}{2R_s\omega_0 C_{tot}} \tag{3.11}$$

The quality factor of a parallel RLC circuit is given as $Q = \frac{R}{\sqrt{L/C}}$ [3]. Therefore, the quality factor of the output circuit at resonant frequency ω_0 is described as

$$Q_{out} = R_{out}C_{out}\omega_0 \tag{3.12}$$

where R_{out} is the parasitic output resistance and C_{out} is the capacitance of the output load. The resonant frequency ω_0 can be expressed in terms of the output capacitance and conductance as

$$\omega_0 = \frac{1}{\sqrt{L_{out}C_{out}}} \tag{3.13}$$

An inductance value of 10 nH and a quality factor of 5 have been used for the output circuit [18].

The definition of noise factor from the previous chapter was given in Eq. (2.23) as

$$F = \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source}$$

In order to find the expression of the noise factor and noise figure, two steps are required. First, all four noise sources need to be identified using thermal noise theory analysis. Second, the contributions of all four noise sources to the output noise power must be computed by using small-signal analysis.

Considering the thermal noise in resistors given by Eq.(2.2), the contributions due to resistor R_s and R_{out} are given by

$$\overline{i_{n,R_s}^2} = 4kT\frac{1}{R_s}\Delta f \tag{3.14}$$

$$\overline{i_{n,R_{out}}^2} = 4kT\frac{1}{R_{out}}\Delta f \tag{3.15}$$

The channel thermal noise mean square value and the induced gate noise mean square value are given according to Eq. (2.7) and Eq. (2.9). Therefore

$$\overline{\iota_{n,d}^2} = 4kT\gamma_{short}g_{d0}\Delta f \tag{3.16}$$

$$\overline{\iota_{n,g}^2} = 4kT\beta_{short}g_g\Delta f \tag{3.17}$$

The significant differences of Eqs. (3.16) and (3.17) from Eqs. (2.7) and (2.9) are that short-channel effects have been taken into account in the expressions in Eqs. (3.16) and (3.17). The parameters γ_{short} and β_{short} are extracted from the noise analysis of short-channel models [30, 38]. Additionally, the conductance of g_{d0} and g_g are also formulated with the contribution of short-channel effects taken into account, which will be discussed in a later section.

With the noise sources calculated, transfer functions using small-signal analysis may be used to find the total output noise power. Once the output noise power is known, the noise figure can be readily expressed. The calculation of the output noise power is based on the small-signal circuit in Figure 3.2. Detailed derivations can be found in Appendix D. In small-signal noise analyses, $\bar{\iota}_{n,R_s}$ is the source resistance thermal noise, $\bar{\iota}_{n,d}$ is the channel thermal noise, $\bar{\iota}_{n,g}$ is the induced gate noise, and $\bar{\iota}_{n,R_{out}}$ is the output resistance thermal noise. The contributions of these four noise sources to the output noise are denoted by $\bar{\iota}_{n,o,R_s}$, $\bar{\iota}_{n,o,d}$, $\bar{\iota}_{n,o,g}$ and $\bar{\iota}_{n,o,R_{out}}$, respectively.

For example, when the output noise due to the input source resistance noise is calculated, other noise sources are removed. The resulting small-signal circuit with only the input source resistance noise is shown in Figure 3.4. The share of the output noise current due to the input source resistance noise can be expressed as,

$$\bar{\iota}_{n,o,R_s} = \frac{g_m}{j2\omega_0 C_{tot}}\bar{\iota}_{n,R_s} \tag{3.18}$$

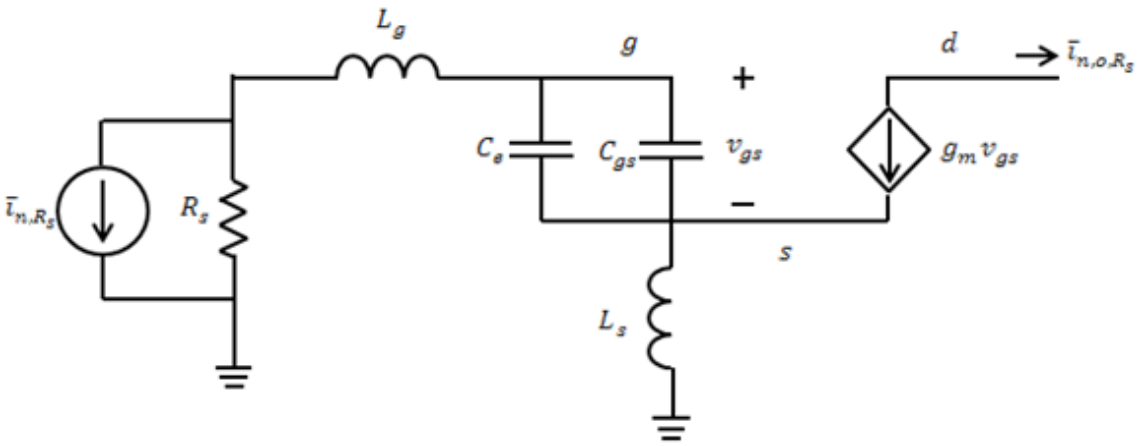


Figure 3.4: Small-signal circuit of the calculation of output noise due to input source resistance noise

Following a similar procedure, the contributions of the other three noise sources to the output noise current are

$$\bar{\imath}_{n,o,d} = -\frac{1}{2}\bar{\imath}_{n,d} \tag{3.19}$$

$$\bar{\imath}_{n,o,g} = \frac{g_m}{j\omega_0 C_{tot}} \frac{1 - jR_s\omega_0 C_{tot}}{j2R_s\omega_0 C_{tot}} \bar{\imath}_{n,g} \tag{3.20}$$

$$\bar{\imath}_{n,o,R_{out}} = \bar{\imath}_{n,R_{out}} \tag{3.21}$$

There is one more component in the output noise current, which is the contribution due to the correlation between the drain current ($\bar{\imath}_{n,d}$) and the induced gate current ($\bar{\imath}_{n,g}$). Calculating the correlation is straightforward because these two noise currents share a common thermal noise origin. The correlation coefficient c is defined by Eq. (2.11). The output noise due to the correlation can be represented as [18]

$$\overline{\imath^2}_{n,o,correlation} = \frac{g_m c}{2\omega_0 C_{tot}} \sqrt{\overline{\imath^2}_{n,g} \cdot \overline{\imath^2}_{n,d}} \tag{3.22}$$

Therefore, the noise factor of the LNA can be rewritten as

$$F = \frac{\overline{\imath^2}_{n,o,R_s} + \overline{\imath^2}_{n,o,d} + \overline{\imath^2}_{n,o,g} + \overline{\imath^2}_{n,o,correlation} + \overline{\imath^2}_{n,o,R_{out}}}{\overline{\imath^2}_{n,o,R_s}} \tag{3.23}$$

By using Eq. (3.14)-(3.22), Eq. (2.10) and Eq. (3.11), the noise factor at resonance is obtained as (see Appendix E)

$$F = 1 + \frac{\frac{1}{4}\gamma g_{d0} + g_m^2\left(\frac{C_{gs}}{C_{tot}}\right)^2\left(Q^2 + \frac{1}{4}\right)\beta\frac{1}{5g_{d0}} + g_m c\left(\frac{C_{gs}}{C_{tot}}\right)\sqrt{\frac{\gamma\cdot\beta}{20}} + \frac{1}{R_{out}}}{g_m^2 R_s Q^2} \tag{3.24}$$

As is shown in Eq. (3.24), the transconductance g_m and the output conductance g_{d0} are the two main model-dependent parameters. The detailed derivations and modeling of the transconductance and the output conductance are described in the next section. Such simple models were constructed by curve fitting monomial expressions to the output conductance g_{d0} and the transconductance g_m data generated from the theoretical equations of short-channel CMOS transistors. These analytical solutions take into consideration velocity saturation and channel-length modulation, which are the predominant short-channel effects.

3.2.2 Monomial Expressions of g_m for Short-channel CMOS Devices

The drain current models and analytical solutions are adapted from Yuan Taur and Tak H. Ning [11]. In their analytical solutions for drain current, velocity saturation and channel-length modulation were taken into account for both triode and saturation regions. A piecewise-continuous velocity saturation model was developed for the drain currents in the triode and saturation regions,

$$I_{dtriode} = \mu_{eff} C_{ox}\left(\frac{W}{L}\right)\cdot\frac{\left(V_{gs} - V_{th}\right)V_{ds} - \left(\frac{m}{2}\right)V_{ds}^2}{1 + (\mu_{eff}V_{ds})/(2v_{sat}L)} \tag{3.25}$$

$$I_{dsat} = \mu_{eff} C_{ox}\left(\frac{W}{L}\right)\frac{\left(V_{gs} - V_{th}\right)^2/(2m)}{1 + \mu_{eff}\left(V_{gs} - V_{th}\right)/(2mv_{sat}L)}\cdot(1 + \lambda V_{ds}) \tag{3.26}$$

where

$$\mu_{eff} = \frac{\mu_0}{1 + \theta\left(V_{gs} - V_{th}\right)} \tag{3.27}$$

$$\theta = \frac{\beta_\theta}{t_{ox}} \tag{3.28}$$

The parameter μ_{eff} in the drain current of Eq. (3.25) and Eq. (3.26) is the effective mobility, which can be estimated as a function of the overdrive voltage as in Eq. (3.27) [3, 22]. The parameter μ_0 is the low field mobility, and θ is the vertical field mobility degradation factor in V^{-1}. The parameter t_{ox} is the oxide thickness and the value of the fitting parameter β_θ is typically 5 to 20 $ÅV^{-1}$. The parameter C_{ox} is the oxide capacitance per unit area, W is the channel width, L is the channel length, $V_{gs} - V_{th}$ is the overdrive voltage, V_{ds} is the drain-to-source voltage, and v_{sat} is the saturation velocity of carriers. Additionally, the channel-length modulation λ is also taken into consideration. The parameter m can be calculated as

$$m = 1 + \frac{\sqrt{\frac{\varepsilon_{si} q N_a}{4\Psi_B}}}{C_{ox}} \tag{3.29}$$

$$\Psi_B = \left(\frac{kT}{q}\right)\ln(N_a/n_i) \tag{3.30}$$

where N_a is the channel doping concentration. The parameter n_i is intrinsic carrier concentration, and its typical value is 1.5×10^{10} cm^{-3} for silicon at room temperature [39].

After the analytical solutions for the drain current are obtained, the transconductance $g_m$can be readily calculated. The transconductance is defined as

$$g_m = \left.\frac{\partial I_{dsat}}{\partial V_{gs}}\right|_{V_{ds}} \tag{3.31}$$

Making use of the drain current in Eq. (3.26), the transconductance for short-channel MOSFETs has the following equivalent form (see Appendix F) of

$$g_m = C_{ox}\mu_0 W v_{sat} \cdot (1 + \lambda V_{ds}) \cdot \frac{\left(4mv_{sat}L(V_{gs} - V_{th}) + (2mv_{sat}L\theta + \mu_0)(V_{gs} - V_{th})^2\right)}{\left(2mv_{sat}L + (2mv_{sat}L\theta + \mu_0)(V_{gs} - V_{th})\right)^2} \quad (3.32)$$

The monomial expression of the transconductance is based on the analytical solution in Eq. (3.32). A simple model with monomial expressions has been obtained to estimate the transconductance (g_m).

$$g_m = A_0 L^{A_1} W^{A_2} I_{ds}^{A_3} \quad (3.33)$$

where g_m is transconductance (S), L is the channel length (m), W is the channel width (m), and I_{ds} is the drain current(A).

In Eq. (3.23), A_0, A_1, A_2, and A_3 are constants estimated from curve fitting. Such curve fitting of a nonlinear equation with multiple input variables is technically challenging and is not likely to be implemented by routine functions available from numerical software (e.g. MATLAB). Therefore, a logarithm transformation can be performed to convert the Eq. (3.33) into a simpler form:

$$\log(g_m) = \log(A_0) + A_1 \cdot \log(L) + A_2 \cdot \log(W) + A_3 \cdot \log(I_{ds}) \quad (3.34)$$

By replacing the old variables (g_m, L, W, I_{ds}) with new variables (g'_m, L', W', I'_{ds}), the following relationships are defined,

$$g'_m = \log(g_m),\ L' = \log(L),$$
$$W' = \log(W), I'_{ds} = \log(I_{ds}) \quad (3.35)$$

As well as replacing the old constants (A_0, A_1, A_2, A_3) with new constants (A'_0, A'_1, A'_2, A'_3), the following relationships are defined,

$$A'_0 = \log(A_0),\ A'_1 = A_1,$$
$$A'_2 = A_2, A'_3 = A_3 \quad (3.36)$$

The aforementioned equation becomes

$$g'_m = A'_0 + A'_1 L' + A'_2 W' + A'_3 g I'_{ds} \tag{3.37}$$

Multiple linear regression analyses, which is a routine function available in MATLAB, can be performed to implement the curve fitting by using this format. In this way, the curve fitting of a monomial expression for the device transconductance is accomplished (see Appendix G for details).

3.2.3 Monomial Expressions of the g_{d0} for Short-channel CMOS Transistors

The analytical solution for the output conductance is derived in this subsection. By definition, g_{d0} is the channel conductance at zero drain bias [23]. In long-channel MOSFETs, g_{d0} is equal to the transconductance g_m in the saturation region. Detailed derivations can be found in Appendix F. The derivation for short-channel MOSFETs is different from the procedure for long-channel MOSFETs. The channel conductance g_d is defined by

$$g_d = \left.\frac{\partial I_{dtriode}}{\partial V_{ds}}\right|_{\mathrm{V_{gs}}} \tag{3.38}$$

where $I_{dtriode}$ is the short-channel triode region drain current in Eq. (3.25).Therefore, the output conductance has the form of

$$g_d = \frac{\mu_{eff} C_{ox} \left(\frac{W}{L}\right) \left[\left(V_{gs} - V_{th}\right) - m V_{ds} - \left(\frac{m}{2}\right) \frac{\mu_{eff}}{2 v_{sat} L} V_{ds}^2\right]}{\left(1 + (\mu_{eff} V_{ds})/(2 v_{sat} L)\right)^2} \tag{3.39}$$

Then the channel conductance at zero bias condition is given by

$$\begin{aligned} g_{d0} &= g_d|_{V_{ds}=0} \\ &= \mu_{eff} C_{ox} \left(\frac{W}{L}\right) V_{od} \end{aligned} \tag{3.40}$$

where V_{od} is the overdrive voltage, which is equal to $\left(V_{gs} - V_{th}\right)$. Details can be found in Appendix F.

A simple model with monomial expressions has also been obtained to estimate the output conductance for short-channel CMOS transistors with the same previous

procedure. Similarly, the output conductance g_{d0} can also be interpreted as a function of channel width, channel length, and the channel current in saturation by applying the MATLAB curve fitting procedure to the following monomial form,

$$g_{d0} = B_0 L^{B_1} W^{B_2} I_{ds}^{B_3} \tag{3.41}$$

where g_{d0} is output conductance at zero bias (S), L is the channel length (m), W is the channel width (m), and I_{ds} is the drain current (A). The parameters B_0, B_1, B_2, and B_3 are constants. The MATLAB script for the curve fitting of the output conductance can be found in Appendix G.

3.2.4 Dimensional Constraints

Minimum and maximum sizes on the transistors are due to lithography limitations and layout area concerns, respectively. Therefore, the dimensional constraints can be expressed as

$$L_{min} \leq L_i \leq L_{max} \tag{3.42}$$

$$W_{min} \leq W_i \leq W_{max} \tag{3.43}$$

Here, the range of L is set to be relatively small, which is close to the minimum feature size of the targeted CMOS technology. The range of W is set to be from 1 μm to 100 μm, which is adequate for channel width requirement.

3.2.5 Input Impedance

To maximize the power delivery to the output load of an LNA, input impedance matching is required to match the real part of the input impedance (i.e. 50 Ω). The imaginary part of the impedance is eliminated and only the real part of the impedance is present.

In Eq.(3.4), the input impedance of the LNA is given by

$$Z_{in} = \frac{g_m}{(C_e + C_{gs})} L_s + j\left[\omega(L_g + L_s) - \frac{1}{\omega(C_e + C_{gs})}\right]$$

Therefore, the impedance matching constraints at the resonant frequency can be obtained as

$$\omega = \omega_0 = \frac{1}{\sqrt{L_{tot} \cdot C_{tot}}} \tag{3.44}$$

$$R_s = \frac{g_m}{C_{tot}} L_s = 50\ \Omega \tag{3.45}$$

3.2.6 Power Dissipation Constraint

Power consumption is very important in wireless communication systems, such as cell phones and other portable devices. For low-noise amplifiers, the power dissipation may be excessive while noise may be minimized. Power dissipation in the LNA can be expressed as

$$P_D = V_{DD} \cdot I_{ds} \tag{3.46}$$

where V_{DD} is the power supply voltage and I_{ds} is the channel current through M_1 in this design. Note that bias circuit current is ignored in this power dissipation approximation. Therefore, the constraint for power dissipation can be expressed as

$$P_D \leq P_{Dmax} \tag{3.47}$$

where P_{Dmax} is chosen according the design specifications.

3.2.7 Other Constraints

An additional capacitor C_e is added to the inductive degeneration LNA circuit as mentioned previously. This capacitor is in parallel to the intrinsic gate capacitance C_{gs} of transistor M_1. Since the sum of C_e and C_{gs} is always greater than C_{gs}, a limitation on the ratio between C_{gs} and the sum of C_e and C_{gs} is given by

$$\frac{C_{gs}}{C_e + C_{gs}} = \frac{C_{gs}}{C_{tot}} \leq 1 \tag{3.48}$$

The intrinsic gate capacitance C_{gs} in saturation is assumed to be:

$$C_{gs} = \frac{2}{3} C_{ox} WL \tag{3.49}$$

In summary, the formulation of geometric programming optimization for short-channel CMOS LNA design has been derived in this chapter. The objective function of the GP optimization is to minimize the noise figure with design constraints, such as device dimensions, input impedance matching, power dissipation and model-dependent parameters (g_m and g_{d0}). Once the formulation is available, the simulation and trade-off analyses are ready to be performed, which will be discussed in the next chapter.

Chapter Four
Application of Geometric Programming to 90 nm and 180 nm CMOS LNAs

In this chapter, geometric programming is applied to the design of short-channel (90 nm and 180 nm) CMOS LNAs with common-source inductive degeneration. First, objective functions and design constraints are expressed in the form of either posynomial functions or monomial functions. Specifically, GP-compatible monomial functions of transconductance and output conductance are obtained for 90 nm and 180 nm CMOS transistors. Next, a MATLAB-based software package for geometric programming, CVX, is used to solve the optimal design of CMOS LNAs. Then, the calculated optimal design parameters are compared with simulations of a numerical simulation tool ADS for electronic circuit design. Finally, tradeoff analyses are performed to examine various design parameters such as input circuit quality factors, noise figure, drain current, and operating frequency.

4.1 Extraction of γ, β, and c

As mentioned in the previous chapter, the power spectral density functions for the channel thermal noise and the induced gate noise are given by the following equations,

$$S_{id} = 4kT\gamma_{short}g_{d0}$$

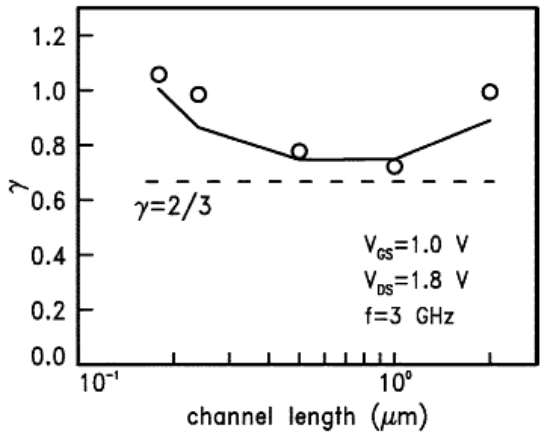
$$S_{ig} = 4kT\beta_{short}g_g$$

where γ_{short} is the white noise factor, β_{short} is the induced gate noise factor, and g_{d0} is the output conductance at zero bias condition ($V_{ds} = 0$). The conductance g_g is given in Chapter Two as

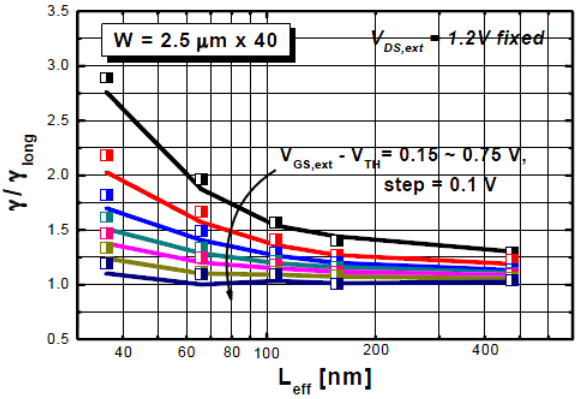
$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}$$

where the intrinsic gate capacitance of transistor $C_{gs} = \frac{2}{3} C_{ox} WL$.

Values of white noise factor γ obtained from experimental measurements and theoretical analyses given in the literature [30, 38] are shown in Figure 4.1.In Figure 4.1(a), the value of γ is close to the 2/3 for channel lengths greater than 1 µm and exhibits an expected increase as channel length decreases due to short-channel effects and increased thermal noise due to parasitic resistances from gate, bulk and source [40]. For longer channel lengths, γ increases due to the non-quasi-static effect. The non-quasi-static effect occurs when higher frequency and longer gate lengths are present [41]. In Figure 4.1(b), the modeled γ/γ_{long} and the experimental results as a function of gate lengths are shown.



(a)



(b)

Figure 4.1: Experimental (markers) and model prediction (solid lines) results of the white noise factor from (a) Scholten *et al.* [30] and (b) Jeon *et al.* [38]

Based on their published results, the white noise factor γ is assumed to be independent of the operating frequencies for moderate frequencies (for example, up to 10GHz), and it is not very sensitive to bias conditions. A comparison between Scholten's and Jeon's experimental results and Deen's analytical solution (Eq. (2.18)) for γ has been made, as shown in Figure 4.2. A very similar trend is observed among the three curves.

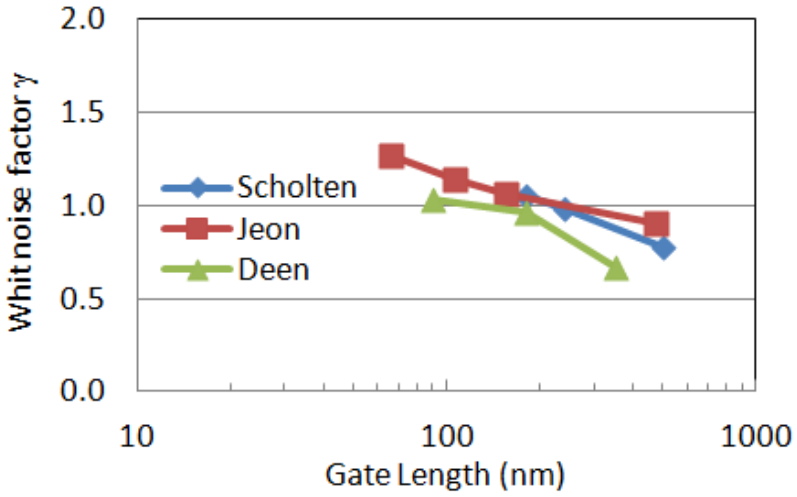


Figure 4.2: White noise factor γ versus gate length

The induced gate noise factor β and correlation coefficient c are adapted from [30, 38]. As shown in Figure 4.3, a significant increase was found for the induced gate noise parameter β due to the contribution from the gate resistance, which consists of the resistance of the vias, the effective resistance of the silicide and the contact resistance between silicide and polysilicon. The value of β is close to 4/3 for long-channel devices, but it is more than twice as large for 180 nm devices. Therefore, a significant increase is expected for shorter devices, e.g., 90 nm devices. The magnitude of the correlation coefficient is 0.395 for long-channel devices [23], and it decreases due to larger γ and β when channel length gets smaller (see Appendix B). Similarly, β and the correlation coefficient c are not dependent on the operating frequencies for moderate frequencies (for example, under 10 GHz), and their variations with bias conditions for strong inversion are not significant.

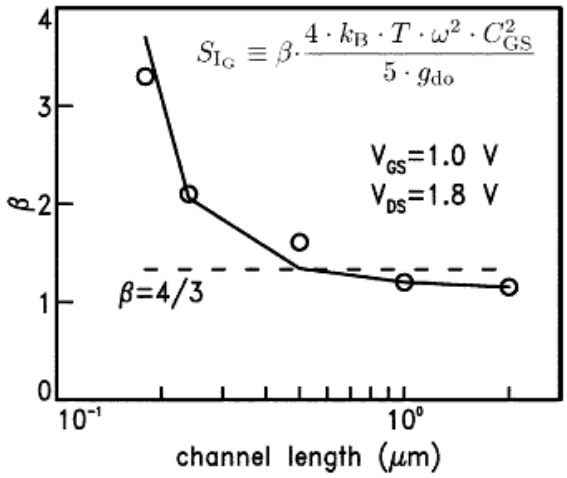


Figure 4.3: Beta factor versus gate channel length [30]

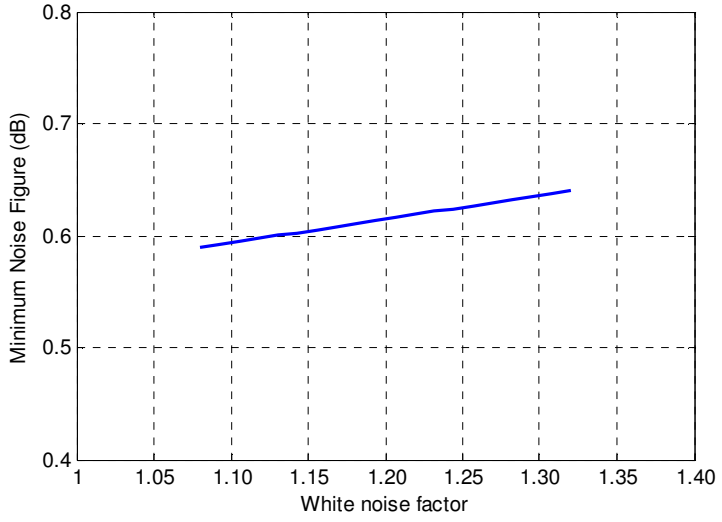
Estimations of white noise factor and the induced gate noise factor at 90 nm gate length have been made based on the experimental results and model predictions from [30, 38], as shown in Table 4.1. The value of c has been measured for 180 nm devices [30], and it equals 0.2 used for the 180 nm model used in this study. The same value has been subsequently estimated for the 90 nm case. The values of the three parameters used in the noise analyses are listed in Table 4.1.

Table 4.1 Noise parameters for the noise analyses for 90 nm and 180 nm CMOS processes

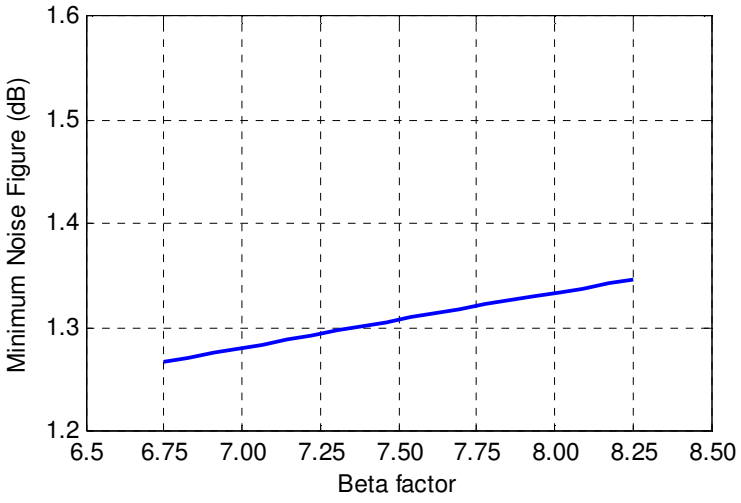
Parameters	90 nm design	180 nm design
White noise factor (γ)	1.2	1.05
Induced gate noise factor (β)	7.5	3.8
Correlation coefficient (c)	0.2	0.2

In order to determine the sensitivity to γ and β on calculation of the minimum noise figure, the effect of varying these parameters was analyzed, as shown in Figures 4.4 and 4.5. When a ±10% variation is applied to γ, a small percentage of variation (around 4%) occurs to the minimum noise figure. Similarly, less than 4% variation occurs on the minimum noise figure when a ±10% change is applied to β. This gives confidence to the

assumption that the parameters γ and β can be modeled as constants for a given technology node.



(a)



(b)

Figure 4.4: (a) Variation of γ factor on minimum noise figure, (b) Variation of β factor on minimum noise figure

4.2 Formulation of GP-compatible Objective Functions and Design Constraints

The process-dependent parameters for calculating the transconductance (g_m) and output conductance (g_{d0}) from analytical solutions are shown in Table 4.2. These parameters for the 90 nm and 180 nm technology nodes are adapted from BSIM3 SPICE models (see Appendix H for details). BSIM3 is the industry-standard MOSFET model for

deep-submicron digital and analog circuit designs from the BSIM Group at the University of California at Berkeley. The geometry ranges specified for these devices for the monomial fitting are given in Table 4.3. Additionally, the bias conditions are chosen to ensure the transistors operate in the saturation regions, e.g., $V_{ds} \geq V_{od}$ shown in Table 4.3. The vertical field mobility degradation factor θ and the channel-length modulation parameter λ have been extracted from the I-V curves generated from SPICE simulations using the aforementioned BSIM3 model parameters (see Appendix I). The calculation of the body effect coefficient m can be found in Appendix F. After monomial expressions for transconductance and output conductance have been determined, the geometric program can be formulated. The objective function and design constraints have been listed as either posynomial or monomial functions.

Table 4.2 Parameters for calculation of g_m and g_{d0} for 90 nm and 180 nm CMOS processes

Parameters	90 nm	180 nm
Electron mobility μ_0	0.0179 m^2/V	0.0288 m^2/V
Electron velocity saturation v_{sat}	1.10×10^5 m/s	9.18×10^5 m/s
Oxide capacitance per unit area C_{ox}	0.014 F/m^2	0.00857 F/m^2
Body effect coefficient m	1.21	1.18
Vertical field mobility degradation factor θ	0.3 V^{-1}	0.2 V^{-1}
Channel-length modulation parameter λ	0.4 V^{-1}	0.3 V^{-1}

Table 4.3 Ranges of devices geometry and bias conditions for calculation of g_m and g_{d0} for 90 nm and 180 nm CMOS processes

Parameters	90 nm	180 nm
Gate length L	0.09 μm $\leq L \leq$ 0.45 μm	0.18 μm $\leq L \leq$ 0.9 μm
Gate width W	1 μm $\leq W \leq$ 100 μm	1 μm $\leq W \leq$ 100 μm
Overdrive voltage V_{od}	0.1 V $\leq V_{od} \leq$ 0.4 V	0.1 V $\leq V_{od} \leq$ 0.5 V
Drain to source voltage V_{ds}	0.5 V $\leq V_{ds} \leq$ 1.0 V	0.6 V $\leq V_{ds} \leq$ 1.2 V

During the calculation of the noise figure for short-channel CMOS LNAs, the monomial expressions of transconductance (g_m) and output conductance (g_{d0}) were obtained by curve fitting one series of data for g_m and one series of data for g_{d0} from the analytical solutions (see Eq. 3.34 and Eq. 3.38) using MATLAB scripts (see Appendix G). As mentioned in the previous chapter, monomial expressions of transconductance (g_m) and output conductance (g_{d0}) are

$$g_m = A_0 L^{A_1} W^{A_2} I_{ds}^{A_3} \quad ; \qquad g_{d0} = B_0 L^{B_1} W^{B_2} I_{ds}^{B_3}$$

The fitting parameters that were determined from the above process are listed in Table 4.4 for both the 90 nm and 180 nm CMOS processes used in this study.

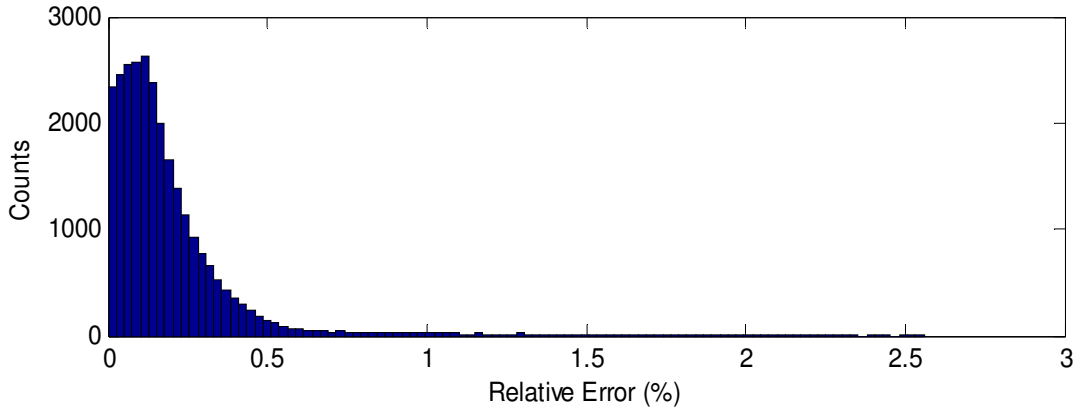
Table 4.4 Fitting parameters of monomial expressions of g_m and g_{d0} for 90 nm and 180 nm CMOS processes

Parameters	90 nm	180 nm
A_0	0.0423	0.0463
A_1	-0.4578	-0.4489
A_2	0.5275	0.5311
A_3	0.4725	0.4689
B_0	0.0091	0.0096
B_1	-0.5637	-0.5595
B_2	0.5305	0.5194
B_3	0.4695	0.4806

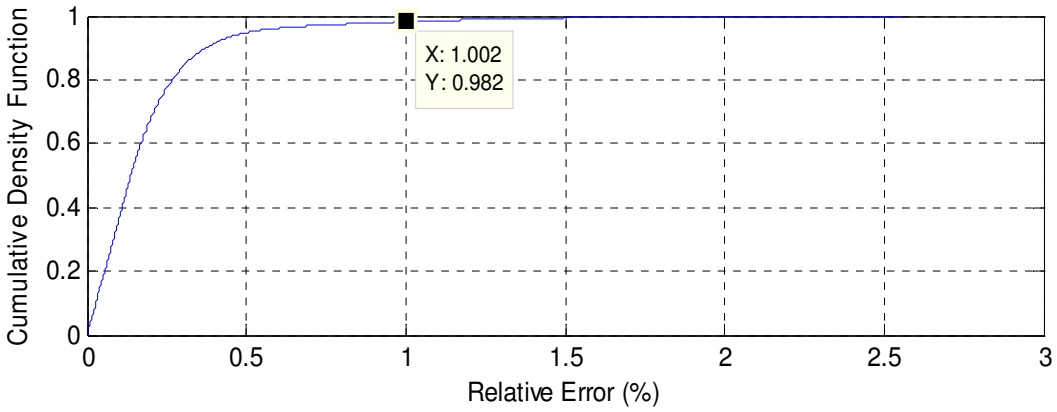
The accuracy of the curve fitting has been examined by comparing the estimated transconductance (g_m) and output conductance (g_{d0}) from the monomial expressions with calculated values from the analytical solutions. The curve fitting results for 180 nm are given in Appendix J.

The curve fitting results for 90 nm are shown in Figures 4.5 and 4.6. The coefficient of determination (R^2 value) for the transconductance curve fitting is 0.9999, indicating that the regression fits extremely well with the data compared with the

analytical solutions in Eq. (3.34). The maximum relative error from curving fitting is about 2.56% (Figure 4.5(a)). Furthermore, 98.2% of the curve fitting data has a relative error less than 1.0% (Figure 4.5(b)).



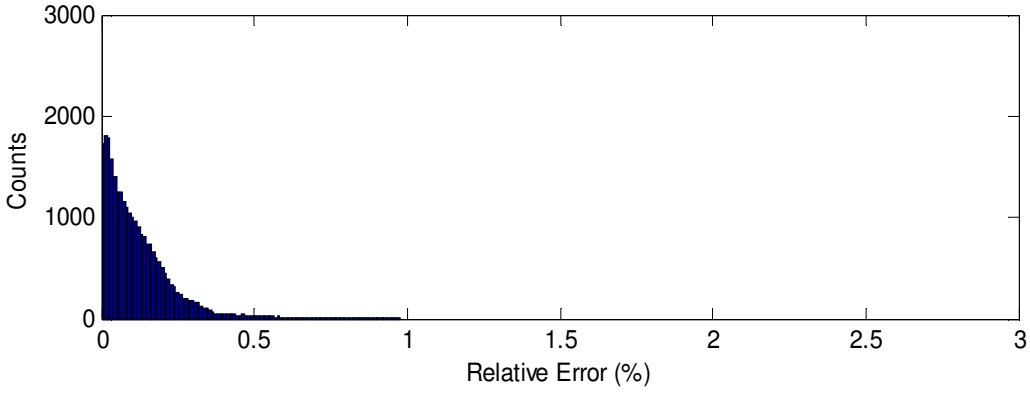
(a)



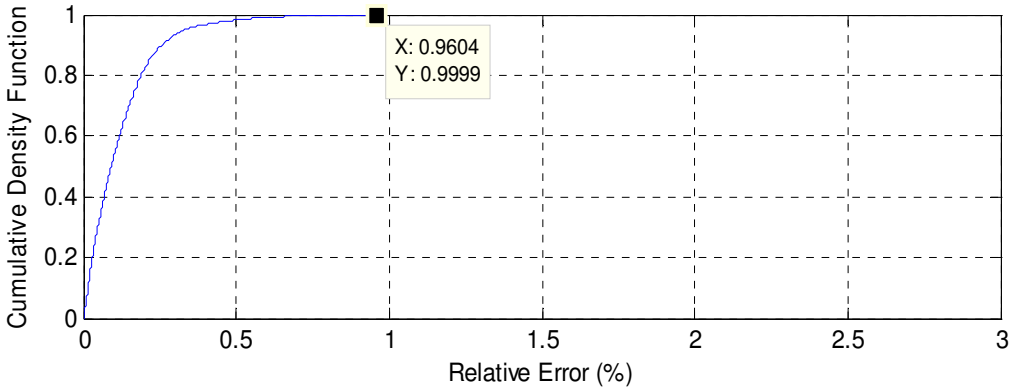
(b)

Figure 4.5: (a) Histogram of relative error for curve fitting of g_m for 90 nm, (b) Cumulative density function of relative error for curve fitting of g_m for 90 nm.

The coefficient of determination for the output conductance is 1.0, suggesting that the curve fitting is close to perfect. The accuracy of curve fitting is shown in Figure 4.6 (a) with a maximum relative error of 0.97%. Moreover, among this curve fitting data, 99.99% of the points have a relative error of less than 0.96% (Figure 4.6 (b)).



(a)



(b)

Figure 4.6: (a) Histogram of relative error for curve fitting of g_{d0} for 90 nm, (b) Cumulative density function of relative error for curve fitting of g_{d0} for 90 nm.

The objective function and design constraints are expressed as either posynomial function or monomial function which is compatible with geometric programming.

The objective function is to minimize Noise Factor F

$$F = 1 + \frac{\frac{1}{4}\gamma g_{d0} + g_m^2\left(\frac{C_{gs}}{C_{tot}}\right)^2\left(Q^2 + \frac{1}{4}\right)\beta\frac{1}{5g_{d0}} + g_m c\left(\frac{C_{gs}}{C_{tot}}\right)\sqrt{\frac{\gamma\cdot\beta}{20}} + \frac{1}{R_{out}}}{g_m^2 R_s Q^2} \tag{4.1}$$

Subject to constraints:

$$L = L_{feature\ size}$$

$$1\ \mu\text{m} \leq W \leq 100\ \mu\text{m}$$

$$
\begin{aligned}
& C_{gs}/C_{tot} \leq 1 \\
& \frac{3}{2} C_{gs}/(C_{ox} WL) = 1 \\
& \frac{(g_m L_s)}{C_{tot}} = 50\ \Omega \\
& I_{ds} \cdot V_{DD} \leq P_{Dmax} \\
& g_m = A_0 L^{A_1} W^{A_2} I_{ds}^{A_3} \\
& g_{d0} = B_0 L^{B_1} W^{B_2} I_{ds}^{B_3}
\end{aligned}
\tag{4.2}
$$

where $L_{feature\ size} = 90$ nm, $V_{DD} = 2$ V and $P_{Dmax} = 1$ mW for the 90 nm process and $L_{feature\ size} = 180$ nm, $V_{DD} = 3$ V and $P_{Dmax} = 1.5$ mW for the 180 nm process.

4.3 A MATLAB-based Software Package for Geometric Programming

To solve the problem summarized in the previous section, CVX, a package for specifying and solving geometric programming problems [42], was used. CVX uses MATLAB as a modeling language for convex optimization and employs standard MATLAB expression syntax to specify objective functions and design constraints. Convex optimization is a special class of mathematical optimization problems including least-squares and linear programming problems. The support of CVX for geometric programming is implemented through a special GP mode. Although geometric programs are not convex, a certain transformation (i.e., log transformation) can be applied to geometric programs to translate them into a solvable convex form. Afterwards, the numerical results can be transferred back to the original problem.

The CVX package has been downloaded from http://cvxr.com/cvx/download/ and installed in an environment of MATLAB 7.6.0 (R2008a) on a Windows 7 Operating System with an Intel Core i3 CPU at 3.13 GHz and 4 GB memory.

A MATLAB script (see Appendix K) was written to implement the geometric programming of objective functions and design constraints as mentioned in the previous section.

4.4 GP Optimization Design Results

The optimal design of CMOS LNAs has been realized by using the CVX software. The average execution time was about 1.45 seconds on a 3.23 GHz PC with 4 GB memory. The resulting optimal design parameters are shown in Table 4.5. In particular, for the 90 nm gate length, the optimal gate width is 22.17 μm, and the corresponding minimum noise figure is 0.6076 dB. The optimal gate width is 27 μm, and the corresponding minimum noise figure is 0.8229 dB for the 180 nm case.

Table 4.5 Optimal design results for low-noise amplifier when input circuit quality factor Q=4 and output circuit quality factor Q_{out}=5

Parameters	90 nm	180 nm
Output conductance (g_{d0})	0.0082 S	0.0063 S
Transconductance (g_m)	0.0069 S	0.0052 S
Gate width (W)	22.172 μm	27.006 μm
Gate length (L)	90 nm	180 nm
P factor ($P = C_{gs}/C_{tot}$)	0.1128	0.1681
Gate intrinsic capacitance (C_{gs})	18.696 fF	27.87 Ff
Additional capacitance (C_e)	0.147 pF	0.13792 pF
Source inductor (L_s)	1.2063 nH	1.5828 nH
Gate inductor (L_g)	25.32 nH	24.943 nH
Drain current (I_{ds})	0.5 mA	0.5 mA
Minimum noise figure (F_{min})	0.6076 dB	0.8229 dB

The results from the optimal design using geometric programming have been compared with results from Agilent's Advanced Design System (ADS) software, a numerical simulation tool used for RF design. The schematic used for the ADS simulation for the 90 nm case is shown in Figure 4.7. A current mirror is implemented to bias transistor M_1 with 0.5 mA. The power supply is set to 2 V and the values of L_g, L_s and C_e are determined by constraints used in the GP optimization. The output parallel RLC values are calculated by the output circuit quality factor, which is given as 5 in this study.

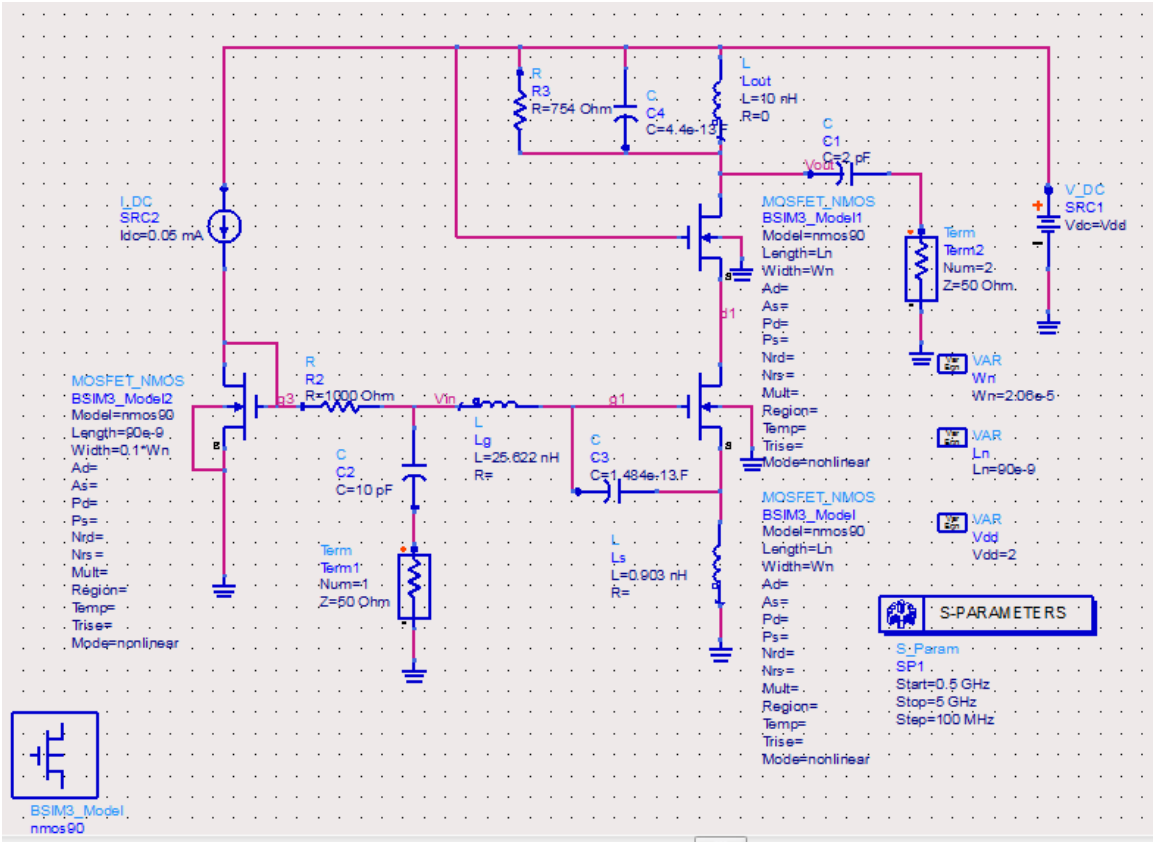


Figure 4.7: Schematic of a CMOS LNA for 90 nm process

Comparison results are shown in Figure 4.8 and 4.9. For the 90 nm design, ADS simulations indicate that the minimum noise figure is 0.2799 dB for a gate width of 27 µm, while the optimal width from the optimization of geometric programming is 22.172 µm with a minimum noise figure of 0.6076 dB. For the 180 nm design, a minimum noise figure of 0.7708 dB was obtained for a gate width of 20 µm, while the optimal width from the optimization of geometric programming is 27.006 µm with a minimum noise figure of 0.8229 dB. As shown in Figure 4.8 and 4.9, the minimum noise figures from numerical simulation are smaller than the minimum noise figures from GP results. These discrepancies are caused by the lack of implementation the excess thermal noise in BSIM3 MOSFET models. The 90 nm design displays relatively larger difference than the 180 nm design, which has confirmed that the excess noise is more significant in shorter channel devices. Such results have suggested that GP is an efficient method to guide the design of short-channel CMOS LNAs.

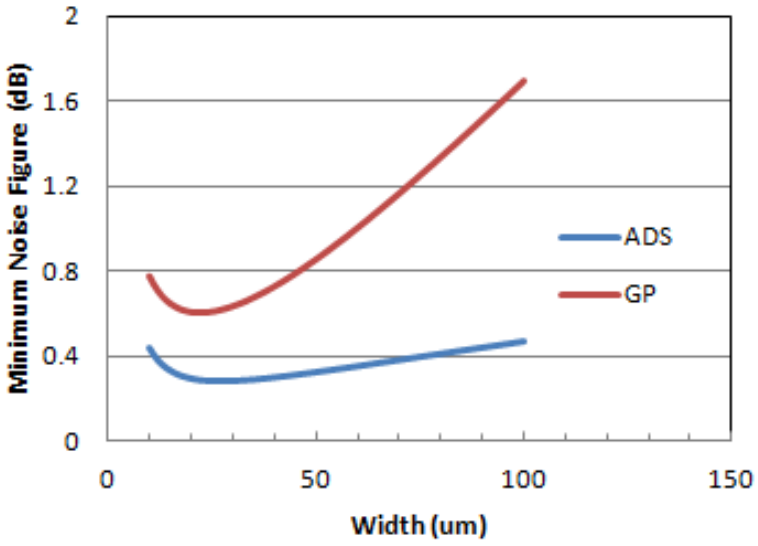


Figure 4.8: Variation of noise figure with different gate width for 90 nm design when Q=4

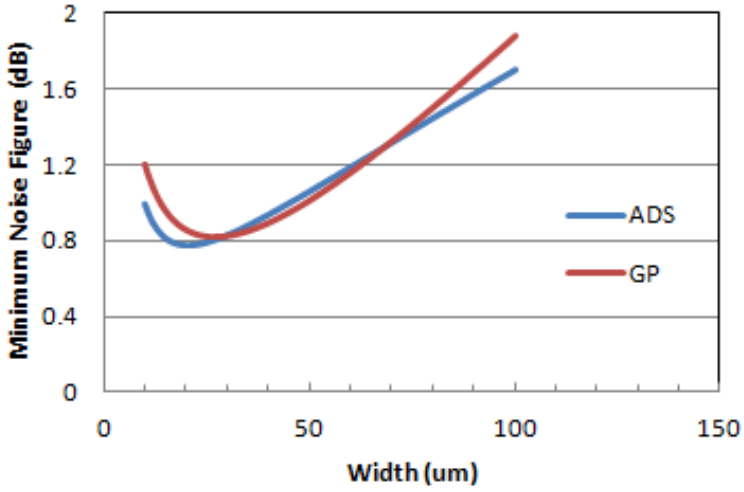


Figure 4.9: Variation of noise figure with different gate width for 180 nm design when Q=4

Optimal results from multiple geometric programming simulations have been obtained by varying the input circuit quality factor. The influence of input circuit quality factor on the minimum noise figure has been demonstrated (Figures 4.10 and 4.11). Same drain current of 0.5 mA has been used for both 90 nm and 180 nm designs for the analyses in Figures 4.10 and 4.11. Minimum noise figure and the corresponding optimal gate width are achieved with different input circuit quality factor.

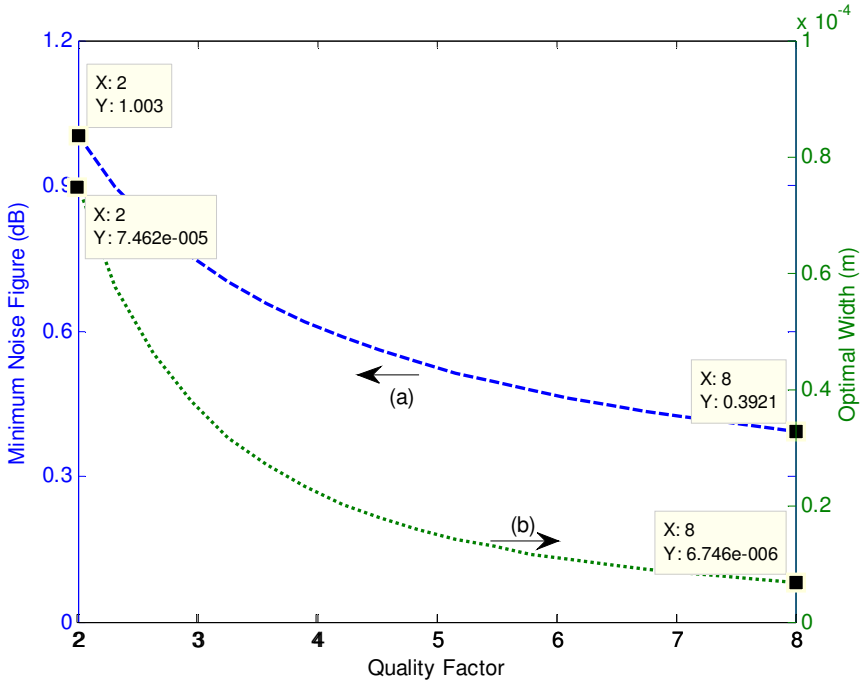


Figure 4.10: (a) Variation of minimum noise figure with different quality factors for 90 nm design, (b) Variation of optimal width with different quality factors for 90 nm design

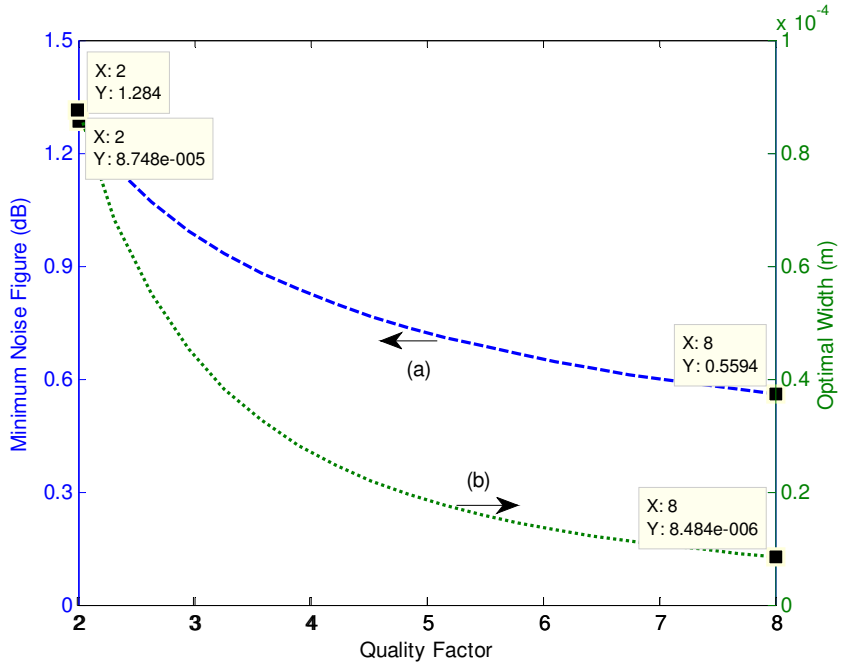


Figure 4.11: (a) Variation of minimum noise figure with different quality factors for 180 nm design, (b) Variation of optimal width with different quality factors for 180 nm design

There is an inverse relationship between input circuit quality factor and minimum noise figure. When the qualify factor increases from 2 to 8, the minimum noise figure decreases from 1 dB to 0.39 dB for the 90 nm design and the minimum noise figure decreases from 1.28 dB to 0.56 dB.

The input circuit quality factor not only affects the minimum noise figure, but also contributes to the optimal width of the low-noise amplifiers. When the qualify factor varies from 2 to 8, the optimal width changes more than 10 times from 74.6 μm to 6.7 μm for 90 nm design and the optimal width changes from 87.5 μm to 8.5 μm. The considerable change in optimal width suggests that input circuit quality factor is a major contributor to optimal width during the design of low-noise amplifiers.

4.5 Trade-off Analyses

Trade-off analyses have been performed for both the 90 nm and 180 nm designs. The impacts of the channel width, input circuit quality factor, drain current, and operation frequency on the noise figures are considered. The trade-off analyses in Figure 4.13, 4.14, 4.17 and 4.18 are under power constraint with a drain current of 0.5 mA. Since very similar trends have been observed for both 90 nm and 180 nm designs, the trade-off analyses for 180 nm are given in Appendix L.

4.5.1 Effect of Input Circuit Quality Factor on the Design of LNAs

As shown in the optimal design results, the influence of the input circuit quality factor on noise figure is very significant. The choice for a reasonable value for the input circuit quality factor becomes very important. It has been observed by Shaeffer and Lee [30] that when the power dissipation and the device geometry are fixed, the best noise performance will be achieved at a certain input circuit quality factor, which is typically close to 4.5 and within the range from 3.5 to 5.5. This analysis was carried out for a 0.6 μm CMOS technology. They also speculate that an increase of this optimal quality factor is expected for shorter devices [3, 29]. This study appears to corroborate this conclusion. For example, when the gate width equals 20 μm and channel length is 90 nm, a series of tradeoff curves have been plotted, which has confirmed that there is an optimal value for input circuit quality factor, and that the optimal quality factors display a small increase which is in the range from 4 to 6, as shown in Figure 4.12 for 90 nm designs.

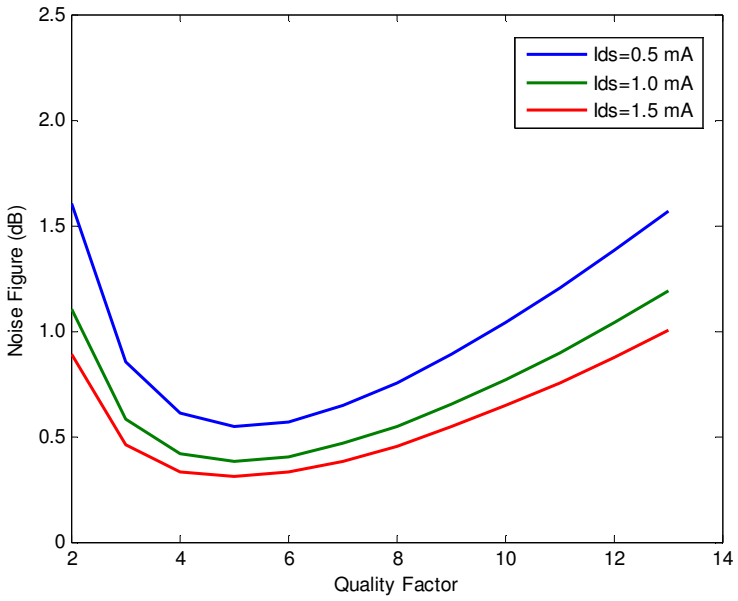


Figure 4.12: Effect of input circuit quality factor on noise figure at different dc drain current (W=20 µm, L=90 nm)

Tradeoff analyses have also shown the influence of the input circuit quality factor on the relationship of the noise figure and the gate width (Figure 4.13).

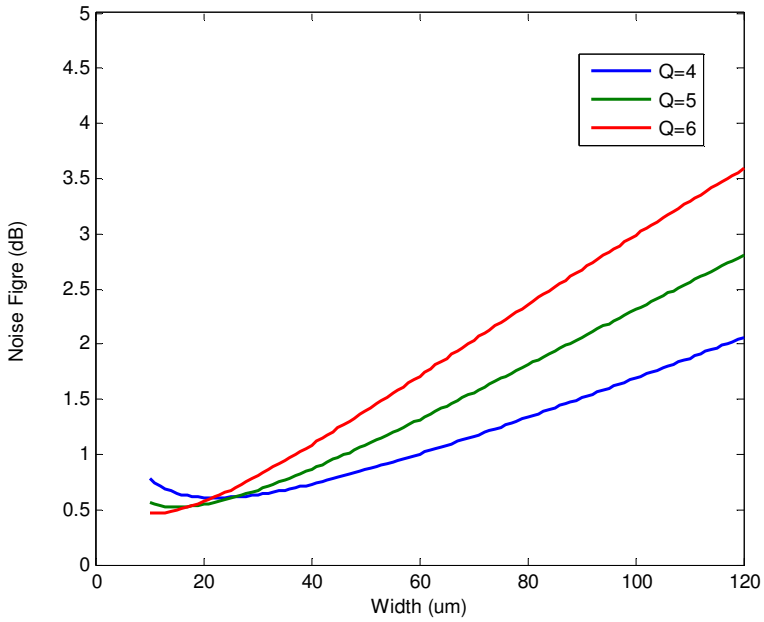


Figure 4.13: Effect of channel width on the noise figure at different input circuit quality factors

The selection of the input circuit quality factor is based on the previous discussion of the optimal values, which are 4, 5 and 6 for this trade-off analysis. The noise figure varies with different channel widths for a fixed input circuit quality factor. When an optimal width is present, a minimum noise figure is achieved. This result is consistent with the previous results from Figures 4.10 and 4.11. Furthermore, such results can be visualized with 3-D plots in Figure 4.14, showing how the input circuit quality factor and channel width affect the noise figure during the design of the low-noise amplifiers. Minimum noise figure can be achieved when either input circuit quality factor or channel width is fixed.

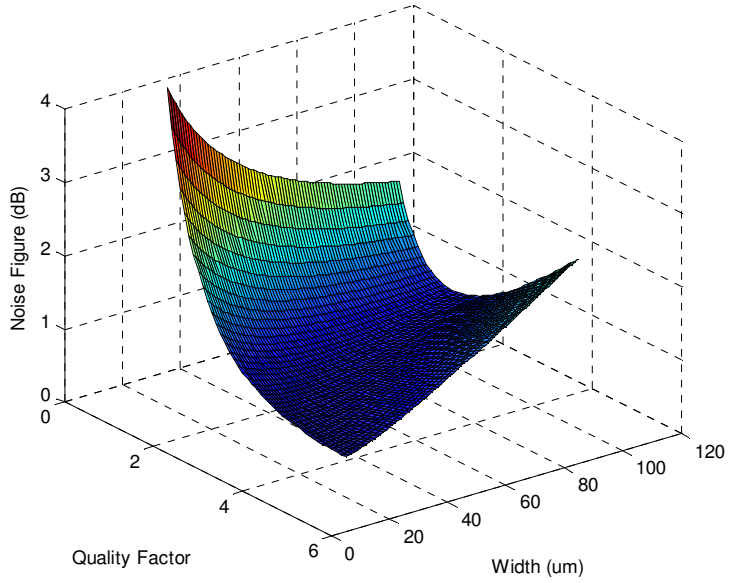


Figure 4.14: Effect of input circuit quality factor and channel width on the noise figure in 3D

4.5.2 Effect of Drain Current and Operational Frequency on the Noise Figure

Drain current appears to have great influence on noise figure when the drain current is at a smaller scale less than 1 mA (Figure 4.15). However, there is not much variation of noise figure when the drain current changes from 1 mA to 4 mA. Such an observation is true at different levels of channel width. This suggests that it is not necessary to have a large drain current in order to reduce the noise figure. A large drain current also means higher power consumption. Therefore, a drain current of 0.5 mA still

offers a small noise figure at relatively low power consumption. Such results can also be easily visualized from 3D plot (Figure 4.16).

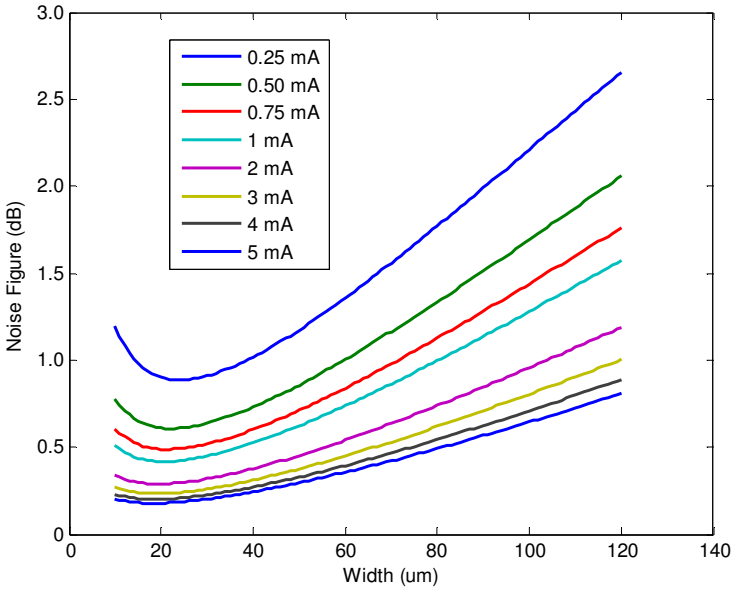


Figure 4.15: Effect of channel width on the noise figure at different drain currents

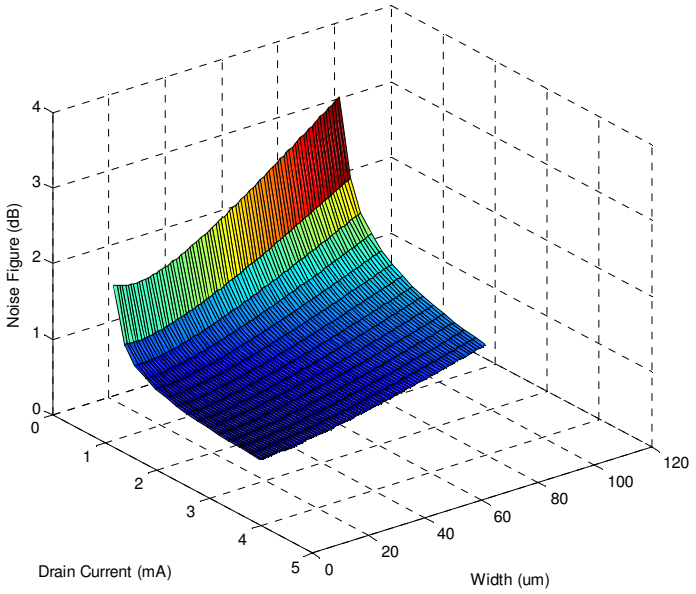


Figure 4.16: Effect of drain current and channel width on the noise figure in 3D

Variation of operational frequency has great influence on the noise figure (Figures 4.17 and 4.18). However, this study focuses on narrowband application. The operating

frequency is fixed at 2.4 GHz. Therefore, the influence of operational frequency on the noise figure is limited.

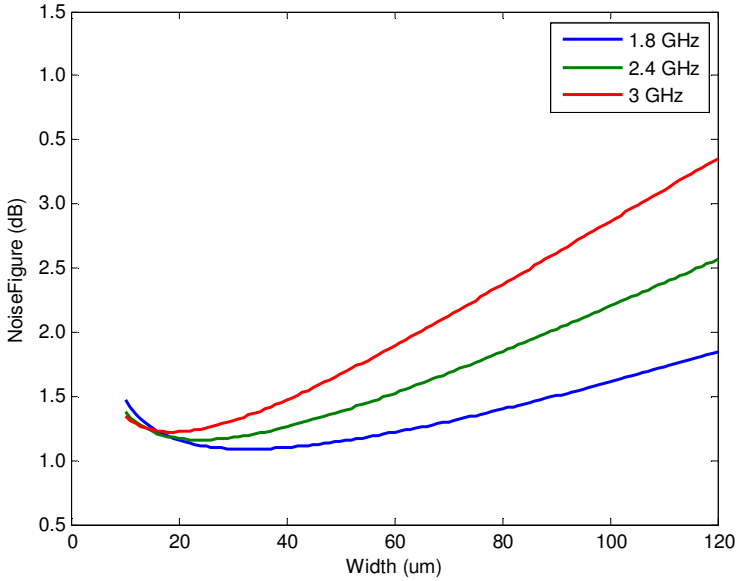


Figure 4.17: Effect of channel width on the noise figure at different frequencies

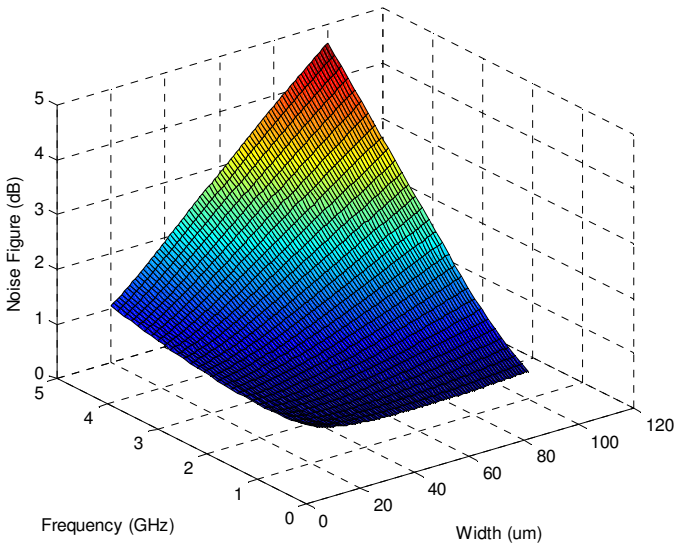


Figure 4.18: Effect of operational frequency and channel width on the noise figure in 3D

In summary, the design optimization of an LNA with inductive degeneration has been conducted by means of geometric programming. Based on the optimal design results and trade-off analyses, several conclusions have been made. First, great efficiency and global optimal results are available using geometric programming. Second, the

variations of noise figure due to design parameters are observed and confirmed with literatures. For example, a minimum noise figure is achievable at the optimal channel width under given power dissipation and input circuit quality factor. The input circuit quality factor has great influences on not only the minimum noise figure but also the optimal width. Based on the trade-off analyses, there seems to be an optimal solution in the LNA design, i.e. a drain current in the range of 0.5 mA to 1 mA with an input circuit quality factor around 5.

Chapter Five
Conclusions and Future Work

In summary, this study has implemented geometric programming to obtain the globally optimal design of short-channel RF CMOS LNAs. First, a framework for noise modeling of short-channel devices has been established by taking consideration of short-channel effects including velocity saturation and channel-length modulation. Then, such a noise model forms the basis for the objective function of geometric programming to minimize the noise figure of CMOS LNAs. In addition, the minimization of noise figure is subjected to design constraints such as input circuit quality factor, power consumption and input impedance match. Finally, geometric programming has been applied to 90nm and 180nm CMOS LNAs to estimate optimal channel width and noise figure. A minimum noise figure is achievable at the optimal channel width when power dissipation is given. An inverse relationship between noise figure and input circuit quality factor has been observed. Such results are consistent with numerical simulation from computer aided design of the circuits. The relationship of noise figure and channel width at a given power dissipation and input circuit quality factor are consistent with numerical simulation from computer aided design of the circuits. Therefore, geometric programming offers an efficient method to guide the optimal design of short-channel CMOS LNAs. With the continuous downscaling of CMOS technologies and constant reduction of turnaround time for designing LNAs nowadays, the geometric programming method provides a high performance advantage over traditional methods for designing CMOS LNAs.

Future work may focus on the enhancement of noise modeling for short-channel CMOS LNAs. For example, the noise contributions from the passive devices, such as the gate inductor (L_g) and the source inductor (L_s) should be taken into consideration for the noise analysis of the CMOS LNAs, and the substrate noise source should be included in future work. Additionally, application of GP optimization for other topologies, such as the shunt-series feedback amplifier, could be included in future work.

References

[1] A. J. Joseph, D. L. Harame, B. Jagannathan *et al.*, "Status and Direction of Communication Technologies - SiGe BiCMOS and RFCMOS," *Proceedings of the IEEE,* vol. 93, no. 9, pp. 1539-1558, 2005.

[2] B. Zhao, H. S. Bennett, J. C. Costa *et al.*, "Future Perspective of RF and Analog/Mixed-Signal Integrated Circuit Technologies for Mobile Communications," *8th International Solid-State and Integrated Circuit Technology* (ICSICT), pp. 1518-1521, 2006.

[3] T. H. Lee, *The Design of CMOS Radio-frequency Integrated Circuits*, 2nd ed., Cambridge, UK: Cambridge University Press 2004.

[4] H. Iwai, "RF CMOS technology," *Proceedings of Radio Science Conference*, Asia-Pacific, pp. 296-298, 2004.

[5] T. H. Lee, "From Oxymoron to Mainstream: The Evolution and Future of RF CMOS," *IEEE International Workshop on Radio-Frequency Integration Technology*, 2007.

[6] C. H. Diaz, D. D. Tang, and J. Y. C. Sun, "CMOS technology for MS/RF SoC," *IEEE Transactions on Electron Devices ,* vol. 50, no. 3, pp. 557-566, 2003.

[7] H. S. Bennett, R. Brederlow, J. C. Costa *et al.*, "Device and technology evolution for Si-based RF integrated circuits," *IEEE Transactions on Electron Devices,* vol. 52, no. 7, pp. 1235-1258, 2005.

[8] P. H. Bonnaud, M. Hammes, A. Hanke *et al.*, "A Fully Integrated SoC for GSM/GPRS in 0.13 μm CMOS," *IEEE International Solid-State Circuits Conference* (ISSCC) , *Digest of Technical Papers*, pp. 1942-1951, 2006.

[9] L. L. Lewyn, T. Ytterdal, C. Wulff *et al.*, "Analog Circuit Design in Nanoscale CMOS Technologies," *Proceedings of the IEEE,* vol. 97, no. 10, pp. 1687-1714, 2009.

[10] A. J. Annema, B. Nauta, R. van Langevelde *et al.*, "Analog circuits in ultra-deep-submicron CMOS," *IEEE Journal of Solid-State Circuits,* vol. 40, no. 1, pp. 132-143, 2005.

[11] Y. Taur, and T. H. Ning, *Fundametals of Modern VLSI Devices*, 2nd ed.: Cambridge University Press, 2009.

[12] R. A. Rutenbar, G. G. E. Gielen, and J. Roychowdhury, "Hierarchical Modeling, Optimization, and Synthesis for System-Level Analog and RF Designs," *Proceedings of the IEEE,* vol. 95, no. 3, pp. 640-669, 2007.

[13] M. d. Hershenson, S. P. Boyd, and T. H. Lee, "Optimal design of a CMOS op-amp via geometric programming," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems ,* vol. 20, no. 1, pp. 1-21, 2001.

[14] S. Boyd, S.-J. Kim, L. Vandenberghe *et al.*, "A tutorial on geometric programming," *Optim Eng,* vol. 8, pp. 67-127, 2007.

[15] M. D. M. Hershenson, A. Hajimiri, S. S. Mohan *et al.*, "Design and optimization of LC oscillators," *International Conference on Computer-Aided Design* (IEEE/ACM), *Digest of Technical Papers*, pp. 65-69,1999.

[16] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd *et al.*, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of Solid-State Circuits ,* vol. 34, no. 10, pp. 1419-1424, 1999.

[17] W.-T. Cheung and N. Wong, "Optimized RF CMOS Low Noise Amplifier Design Via Geometric Programming," *International Symposium on Intelligent Signal Processing and Communications* (ISPACS), pp. 423-426, 2006.

[18] P. Andreani and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 48, no. 9, pp. 835-841, 2001.

[19] J. B. Johnson, "Thermal agitation of electricity in conductors," *Nature,* vol. 119, no. 2984, pp. 50-1, 1927.

[20] J. B. Johnson, "Thermal agitation of electricity in conductors," *Physical review,* vol. 32, pp. 97-109, 1928.

[21] H. Nyquist, "Thermal agitation of electric charge in conductors," *Physical review,* vol. 32, no. 7, pp. 110-113, July, 1928.

[22] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed., New York: Oxford University Press, 2003.

[23] A. van der Ziel, *Noise in Solid State Devices and Circuits*, New York: John Wiley & Sons, 1986.

[24] M. J. Deen, C. Chih-Hung, S. Asgaran *et al.*, "High-Frequency Noise of Modern MOSFETs: Compact Modeling and Measurement Issues," *IEEE Transactions on Electron Devices,* vol. 53, no. 9, pp. 2062-2081, 2006.

[25] T. Ytterdal, Y. Cheng, and T. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design*: John Wiley & Sons, 2003.

[26] K. Lee, M. Shur, T. Fjeldly *et al.*, *Semiconductor Device Modeling for VLSI*, Englewood Cliffs: Prentice Hall, 1993.

[27] F. M. Klaassen, and J. Prins, "Thermal noise of MOS transitors," *Philips Res. Rep.,* vol. 22, pp. 505-514, 1967.

[28] A. J. Scholten, R. van Langevelde, L. F. Tiemeijer *et al.*, "Compact modeling of noise in CMOS," *IEEE Custom Integrated Circuits Conference* (CICC), pp. 711-716, 2006.

[29] D. K. Shaeffer, and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier," *IEEE Journal of Solid-State Circuits,* vol. 32, no. 5, 1997.

[30] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde *et al.*, "Noise modeling for RF CMOS circuit simulation," *IEEE Transactions on Electron Devices,* vol. 50, no. 3, pp. 618-632, 2003.

[31] K. Han, J. Gil, S.-S. Song *et al.*, "Complete high-frequency thermal noise modeling of short-channel MOSFETs and design of 5.2-GHz low noise amplifier," *IEEE Journal of Solid-State Circuits,* vol. 40, no. 3, pp. 726-735, 2005.

[32] "http://www.semiconductors.philips.com/Philips_Models/."

[33] J. C. J. Paasschens, A. J. Scholten, and R. van Langevelde, "Generalizations of the Klaassen-Prins equation for calculating the noise of semiconductor devices," *IEEE Transactions on Electron Devices,* vol. 52, no. 11, pp. 2463-2472, 2005.

[34] K. Han, H. Shin, and K. Lee, "Analytical Drain Thermal Noise Current Model Valid for Deep Submicron MOSFETs," *IEEE Transactions on Electron Devices,* vol. 51, no. 2, pp. 261-269, Feb., 2004.

[35] W. Shockley, J. A. Copeland, and R. P. James, "The impedance field method of noise calculation in active semiconductor devices, " *Quantum theory of atoms, molecules and solid state*, pp. 537-563, New York: Academic Press, 1966.

[36] B. J. Sheu, D. L. Scharfetter, P. K. Ko *et al.*, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE Journal of Solid-State Circuits ,* vol. 22, no. 4, pp. 558-566, 1987.

[37] J. Jeon, J. D. Lee, B.-G. Park *et al.*, "An analytical channel thermal noise model for deep-submicron MOSFETs with short channel effects," *Solid-State Electronics,* vol. 51, pp. 1034-1038, 2007.

[38] J. Jeon, B.-G. Park, and H. Shin, "Investigtion of the thermal noise factor in nanoscale MOSFETs," *Journal of Semiconductor Technology and Science,* vol. 10, no. 3, pp. 225-231, Sep., 2010.

[39] B. G. Streetman, and S. K. Banerjee, *Solid state electronic devices*, 6th ed.: Prentice Hall, 2005.

[40] M. J. Deen, C. H. Chen, and Y. Cheng, "MOSFET modeling for low noise , RF circuit design," *Proceedings of the IEEE Custom Integrated Circuits Conf.* (CICC), pp. 201-208, 2002.

[41] E. Gondro, O. Kowarik, G. Knoblinger *et al.*, "When do we need Non-Quasistatic CMOS RF-Models?," *IEEE Custom Integrated Circuit Conference* (CICC), San Diego, California, USA, 2001, pp. 377-380, 2001.

[42] M. Grant, and S. Boyd. "CVX: Matlab software for disciplined convex programming, version 1.21, " http://cvxr.com/cvx/.

[43] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed., New York, NY: McGraw-Hill, 2000.

Appendix A

This appendix shows how channel thermal noise power spectral density can be expressed as a white noise gamma formula for long-channel devices.

The power spectral density of channel thermal noise S_{id} is given in Eq. (2.5) as

$$S_{i_d} = \frac{4kT}{L^2 I_d} \int_0^{V_{ds}} g^2(V) \cdot dV$$

where I_d is the drain current, L is the gate length and $g(V)$ is the local output conductivity. For long-channel devices, the drain current in saturation is

$$I_d = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L} V_{od}^2 \qquad (A.1)$$

where the overdrive voltage $V_{od} = V_{gs} - V_{th}$.

With the gradual channel approximation, the local output conductance at position x can be expressed as

$$g(V(x)) = \mu_0 C_{ox} W \left(V_{gs} - V_{th} - V(x) \right) \qquad (A.2)$$

where $V(x)$ is the difference in electron quasi-Fermi potential in the inversion layer and the hole quasi-Fermi potential in the bulk at position x.

Therefore, S_{id} for long-channel can be rewritten as using $V_{ds} = V_{od}$ (no channel-length modulation in saturation region)

$$S_{i_d} = \frac{4kT}{L^2 \left(\frac{1}{2} \mu_0 C_{ox} \frac{W}{L} V_{od}^2 \right)} \int_0^{V_{od}} \left(\mu_0 C_{ox} W (V_{od} - V) \right)^2 \cdot dV$$

$$= \frac{4kT (\mu_0 C_{ox} W)^2}{L^2 \left(\frac{1}{2} \mu_0 C_{ox} \frac{W}{L} V_{od}^2 \right)} \int_0^{V_{od}} (V_{od} - V)^2 \cdot dV$$

$$= 4kT \frac{2\mu_0 C_{ox} W}{L V_{od}^2} \cdot \frac{1}{3} (V_{od} - V)^3 \Big|_0^{V_{od}}$$

$$= 4kT \cdot \frac{2}{3}\frac{\mu_0 C_{ox} W}{L} V_{od} \qquad (A.3)$$

where $\frac{\mu_0 C_{ox} W}{L} V_{od}$ is the expression of g_{d0} (see Appendix F). Therefore, the power spectral density of channel thermal noise can be written as

$$S_{i_d} = 4kT \cdot \gamma_{long} g_{d0} \qquad (A.4)$$

where the white noise gamma factor γ_{long} equals 2/3 for long-channel devices.

Appendix B

The calculation of correlation coefficient c is described in this appendix. Since the induced gate noise is correlated with the drain thermal noise, the correlation coefficient is defined as [23]

$$c = \frac{\overline{\iota_{ng} \cdot \iota_{nd}^{*}}}{\sqrt{\overline{\iota_{ng}^{2}} \cdot \overline{\iota_{nd}^{2}}}} \tag{B.1}$$

where $\overline{\iota_{ng} \cdot \iota_{nd}^{*}}$ is the spectrum of the crosscorrelation of the drain thermal noise and the induced gate noise, $\overline{\iota_{n,d}^{2}}$ is the spectrum of the drain thermal noise and $\overline{\iota_{n,g}^{2}}$ is the spectrum of the induced gate noise. In long-channel, they are given as [23]

$$\overline{\iota_{ng} \cdot \iota_{nd}^{*}} = 4kT \cdot \frac{1}{9} j\omega (C_{ox} WL) \cdot \Delta f \tag{B.2}$$

$$\overline{\iota_{n,d}^{2}} = 4kT\gamma_{long} g_{d0} \Delta f \tag{B.3}$$

$$\overline{\iota_{n,g}^{2}} = 4kT\beta_{long} g_{g} \Delta f \tag{B.4}$$

where

$$g_{g} = \frac{\omega^{2} C_{gs}^{2}}{5 g_{d0}} \tag{B.5}$$

$$C_{gs} = \frac{2}{3} C_{ox} WL \tag{B.6}$$

By substitution of Eq. (B.2)- (B.6) into Eq. (B.1), the correlation coefficient c for long-channel can be calculated as

$$c = \frac{4kT \cdot \frac{1}{9} j\omega (C_{ox} WL) \cdot \Delta f}{\sqrt{4kT\beta_{long} \frac{\omega^{2} C_{gs}^{2}}{5 g_{d0}} \Delta f \cdot 4kT\gamma_{long} g_{d0} \Delta f}}$$

$$= \frac{\frac{1}{9}j}{\frac{2}{3}\sqrt{\frac{1}{5}\beta_{long} \cdot \gamma_{long}}}$$

$$= \frac{1}{6\sqrt{\frac{1}{5}\beta_{long} \cdot \gamma_{long}}}j \qquad (B.7)$$

Substituting β_{long} and γ_{long} with their corresponding long-channel values of 4/3 and 2/3, yields

$$c = \frac{1}{6\sqrt{\frac{1}{5} \cdot \frac{4}{3} \cdot \frac{2}{3}}}j = 0.395j \qquad (B.8)$$

Appendix C

The calculation of the input impedance is needed to specify the impedance matching requirements for LNAs design. The equivalent circuit for calculating the input impedance of the LNA is shown in Figure C-1.

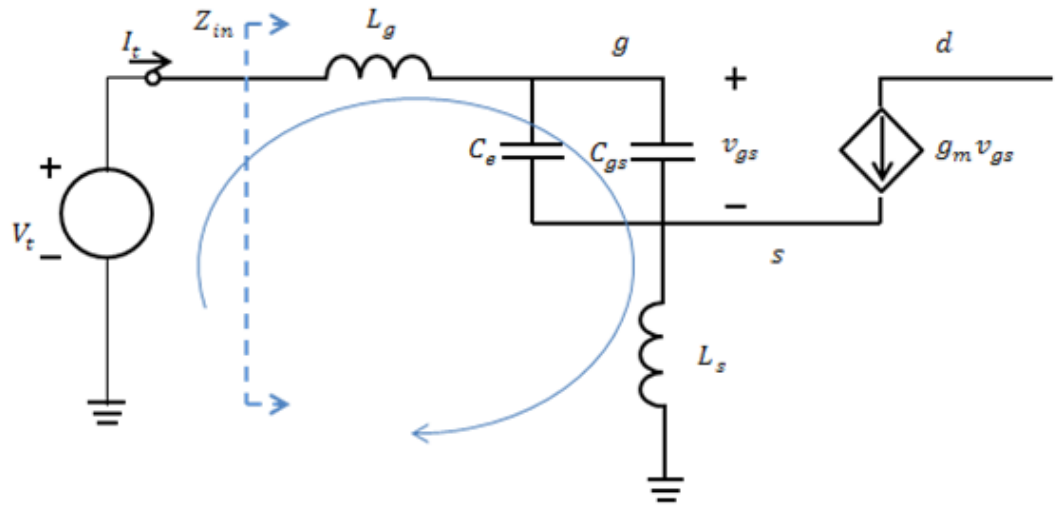


Figure C-1: Equivalent circuit of input impedance calculation

After applying a test voltage V_t and calculating the current I_t, the input impedance can be determined by

$$Z_{in} = \frac{V_t}{I_t}$$

$$= \frac{I_t\left(j\omega L_g + \frac{1}{j\omega(C_e+C_{gs})}\right) + \left(I_t + g_m V_{gs}\right)j\omega L_s}{I_t} \qquad (C.1)$$

where

$$v_{gs} = I_t \frac{1}{j\omega(C_e + C_{gs})} \qquad (C.2)$$

Therefore, the input impedance can be expressed as

$$Z_{in} = \frac{I_t\left(j\omega L_g + \frac{1}{j\omega(C_e+C_{gs})}\right) + \left(I_t + g_m\left(I_t \frac{1}{j\omega(C_e+C_{gs})}\right)\right) j\omega L_s}{I_t}$$

$$= \left(j\omega L_g + \frac{1}{j\omega(C_e + C_{gs})}\right) + \left(1 + g_m\left(\frac{1}{j\omega(C_e + C_{gs})}\right)\right) j\omega L_s$$

$$= \frac{1}{j\omega\left(C_e + C_{gs}\right)} + j\omega(L_g + L_s) + \frac{g_m}{\left(C_e + C_{gs}\right)} L_s$$

$$= \frac{g_m}{\left(C_e + C_{gs}\right)} L_s + j\left[\omega(L_g + L_s) - \frac{1}{\omega\left(C_e + C_{gs}\right)}\right] \qquad (C.3)$$

At the resonant frequency ω_0, the input impedance should be purely resistive and equals the source resistance for the maximum power delivery.

$$\frac{g_m}{\left(C_e + C_{gs}\right)} L_s = \frac{g_m}{C_{tot}} L_s = R_s \qquad (C.5)$$

The imaginary term of the input impedance equal to zero yields,

$$\omega(L_g + L_s) = \frac{1}{\omega\left(C_e + C_{gs}\right)} \qquad (C.6)$$

The equations required to obtain an input impedance match at the resonant frequency are,

$$\frac{g_m}{C_{tot}} L_s = R_s$$

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)\left(C_e + C_{gs}\right)}} = \frac{1}{\sqrt{L_{tot} \cdot C_{tot}}} \qquad (C.7)$$

Appendix D

This appendix gives the detailed derivations for calculating the contributions of the output noise current due to the input noise sources. Four noise sources, which are input source resistance noise, channel thermal noise, induced gate noise and output resistance noise, will be discussed in the following sections.

D.1 Contribution of Input Source Resistance

The contribution of output noise current due to the noise current of input source resistance $\bar{\imath}_{n,o,R_s}$ can be obtained using the following small-signal circuit.

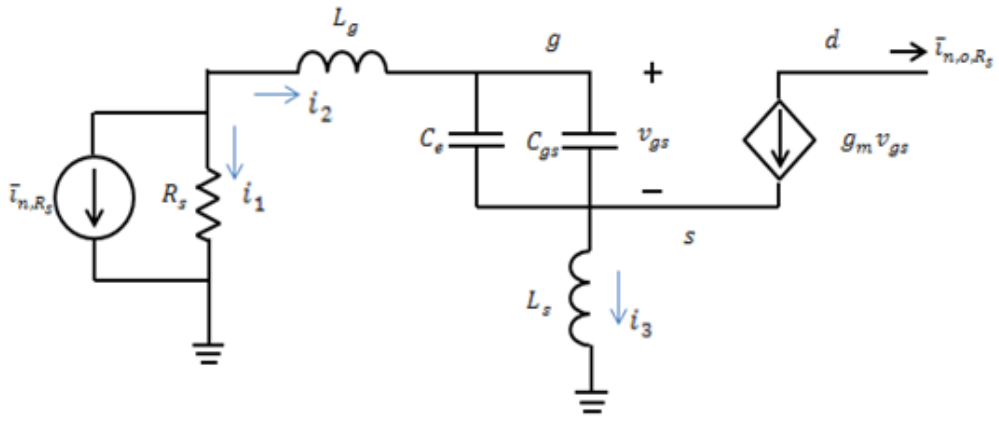


Figure D-1: Small-signal circuit for calculating output noise due to the noise current of input source resistance

At the resonant frequency ω_0, the current and voltage relationship are given by

$$v_{gs} = i_2 \cdot \frac{1}{j\omega_0(C_e + C_{gs})} \tag{D.1}$$

$$i_1 + i_2 + \bar{\imath}_{n,R_s} = 0 \tag{D.2}$$

$$i_1 R_s = i_2 \left(j\omega_0 L_g + \frac{1}{j\omega_0(C_e + C_{gs})} \right) + i_3\, j\omega_0 L_s \tag{D.3}$$

$$i_3 = i_2 + g_m v_{gs} \tag{D.4}$$

$$\bar{\imath}_{n,o,R_s} = -g_m v_{gs} \tag{D.5}$$

Using Eq. (D.1, (D.2), and (D.5), current components can be rewritten as

$$i_1 = -j\omega_0(C_e + C_{gs})v_{gs} - \bar{\imath}_{n,R_s} \qquad (D.6)$$

$$i_2 = j\omega_0(C_e + C_{gs})v_{gs} \qquad (D.7)$$

$$i_3 = j\omega_0(C_e + C_{gs})v_{gs} + g_m v_{gs} \qquad (D.8)$$

Then, substituting above expressions into Eq. (D.3), yields v_{gs} in terms of $\bar{\imath}_{n,R_s}$

$$v_{gs} = -\frac{1}{2j\omega_0(C_e + C_{gs})}\bar{\imath}_{n,R_s} \qquad (D.9)$$

Therefore,

$$\bar{\imath}_{n,o,R_s} = \frac{g_m}{2j\omega_0(C_e + C_{gs})}\bar{\imath}_{n,R_s} \qquad (D.10)$$

D.2 Contribution of the Channel Thermal Noise Current

The contribution of output noise current due to the channel thermal noise current $\bar{\imath}_{n,o,d}$ can be found using the following small-signal circuit.

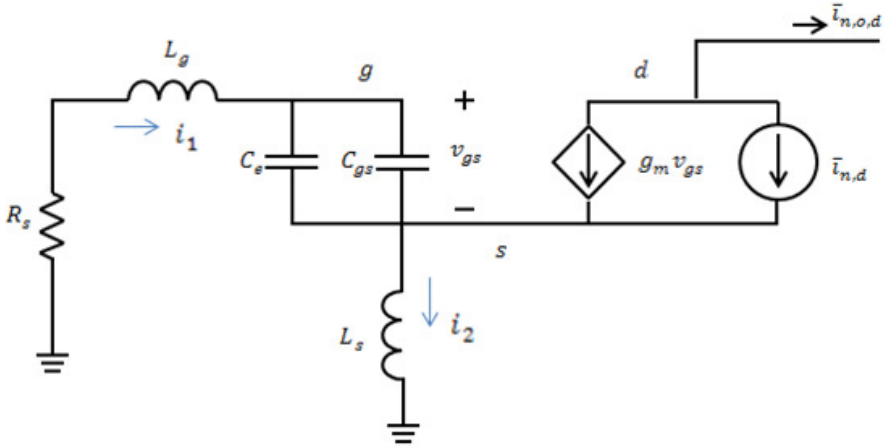


Figure D-2: Small-signal circuit for calculating output noise due to channel thermal noise current

At the resonant frequency ω_0, the current and voltage relationship are given by

$$v_{gs} = i_1 \cdot \frac{1}{j\omega_0(C_e + C_{gs})} \quad (D.11)$$

$$i_1 + g_m v_{gs} + \bar{\imath}_{n,d} = i_2 \quad (D.12)$$

$$i_1 \left(R_s + j\omega_0 L_g + \frac{1}{j\omega_0(C_e + C_{gs})} \right) + i_2\, j\omega_0 L_s = 0 \quad (D.13)$$

$$\bar{\imath}_{n,o,d} = -g_m v_{gs} - \bar{\imath}_{n,d} \quad (D.14)$$

Using Eq. (D.11) and (D.12), i_1 and $i_2$can be rewritten as

$$i_1 = j\omega_0(C_e + C_{gs})v_{gs} \quad (D.15)$$

$$i_2 = j\omega_0(C_e + C_{gs})v_{gs} + g_m v_{gs} + \bar{\imath}_{n,d} \quad (D.16)$$

Then, substituting the above expression of i_1 and i_2 into Eq. (D.13), yields v_{gs} in terms of $i_{n,d}$

$$v_{gs} = -\frac{j\omega_0 L_s}{1 - \omega_0^2(C_e + C_{gs})(L_g + L_s) + j\omega_0 R_s(C_e + C_{gs}) + j\omega_0 g_m L_s} \bar{\imath}_{n,d} \quad (D.17)$$

Since

$$\omega_0^2(C_e + C_{gs})(L_g + L_s) = 1$$

$$\frac{g_m L_s}{(C_e + C_{gs})} = R_s$$

then,

$$v_{gs} = -\frac{1}{2g_m} \bar{\imath}_{n,d} \quad (D.18)$$

Therefore,

$$\bar{\imath}_{n,o,d} = -\frac{1}{2} \bar{\imath}_{n,d} \quad (D.19)$$

D.3 Contribution of the Induced Gate Noise Current

The contribution of output noise current due to the induced gate noise current can be found using the following small-signal circuit.

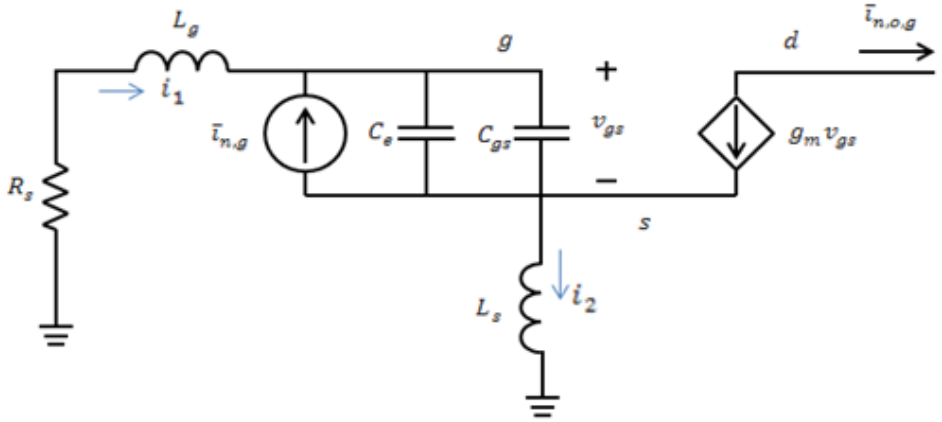


Figure D-3: Small-signal circuit for calculating output noise due to induced gate noise current

At the resonant frequency ω_0, the current and voltage relationship are given by

$$i_1 + g_m v_{gs} = i_2 \qquad (D.20)$$

$$i_1 + \bar{\imath}_{n,g} = v_{gs} j\omega_0 (C_e + C_{gs}) \qquad (D.21)$$

$$i_1 \left(R_s + j\omega_0 L_g\right) + v_{gs} + i_2 j\omega_0 L_s = 0 \qquad (D.22)$$

$$\bar{\imath}_{n,o,g} = -g_m v_{gs} \qquad (D.23)$$

Using Eq. (D.21) and (D.22), the current components can be rewritten as,

$$i_1 = v_{gs} j\omega_0 (C_e + C_{gs}) - \bar{\imath}_{n,g} \qquad (D.24)$$

$$i_2 = -\frac{\left(v_{gs} j\omega_0 (C_e + C_{gs}) - \bar{\imath}_{n,g}\right)\left(R_s + j\omega_0 L_g\right) + v_{gs}}{j\omega_0 L_s} \qquad (D.25)$$

Solving Eq. (D.24) and (D.25), it yields v_{gs} in terms of $\bar{\imath}_{n,g}$

$$v_{gs} = \frac{R_s + j\omega_0 (L_g + L_s)}{1 - \omega_0^2 (C_e + C_{gs})(L_g + L_s) + j\omega_0 R_s (C_e + C_{gs}) + j\omega_0 g_m L_s} \cdot \bar{\imath}_{n,g} \qquad (D.26)$$

Since

$$\omega_0^2(C_e + C_{gs})(L_g + L_s) = 1$$

$$\frac{g_m L_s}{(C_e + C_{gs})} = R_s$$

then,

$$v_{gs} = \frac{1}{j\omega_0(C_e + C_{gs})} \frac{j\omega_0 R_s(C_e + C_{gs}) - 1}{2j\omega_0 R_s(C_e + C_{gs})} \cdot \bar{\imath}_{n,g} \qquad (D.27)$$

Substituting the above expression of v_{gs} into Eq. (D.23), yields

$$\bar{\imath}_{n,o,g} = \frac{g_m}{j\omega_0(C_e + C_{gs})} \frac{1 - j\omega_0 R_s(C_e + C_{gs})}{2j\omega_0 R_s(C_e + C_{gs})} \cdot \bar{\imath}_{n,g} \qquad (D.28)$$

D.4 Contribution of the Output Resistance

The contribution of output noise current due to the noise current of the output resistance can be obtained using the following small-signal circuit.

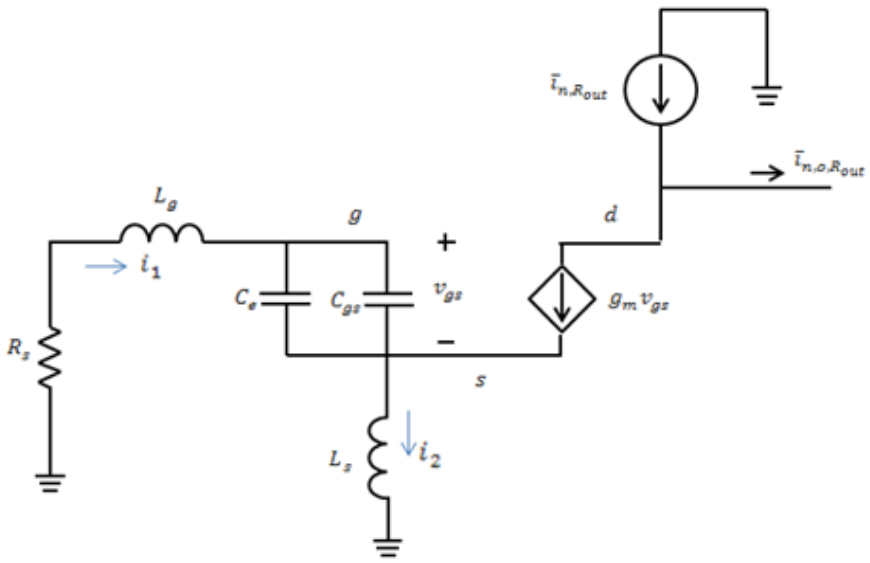


Figure D-4: Small-signal circuit for calculating output noise due to the noise current of the output resistance

At the resonant frequency ω_0, the current and voltage relationship are given by

$$i_1 + g_m v_{gs} = i_2 \tag{D.29}$$

$$i_1\left(R_s + j\omega_0 L_g + \frac{1}{j\omega_0(C_e + C_{gs})}\right) + i_2 j\omega_0 L_s = 0 \tag{D.30}$$

$$v_{gs} = i_1 \frac{1}{j\omega_0(C_e + C_{gs})} \tag{D.31}$$

$$\bar{\imath}_{n,o,R_{out}} + g_m v_{gs} = \bar{\imath}_{n,R_{out}} \tag{D.32}$$

Using Eq. (D.30), the current component i_2 can be rewritten as

$$i_2 = \frac{\left(R_s + j\omega_0 L_g + \frac{1}{j\omega_0(C_e+C_{gs})}\right)}{-j\omega_0 L_s} i_1 \tag{D.33}$$

Substituting the above expression of i_2 into Eq. (D.29), yields i_1 in the form of

$$i_1 = \frac{-g_m j\omega_0 L_s}{j\omega_0 L_s + R_s + j\omega_0 L_g + \frac{1}{j\omega_0(C_e+C_{gs})}} v_{gs}$$

$$= \frac{g_m \omega_0^2 L_s(C_e + C_{gs})}{-\omega_0^2(L_s + L_g)(C_e + C_{gs}) + R_s j\omega_0(C_e + C_{gs}) + 1} v_{gs} \tag{D.34}$$

Since

$$\omega_0^2(C_e + C_{gs})(L_g + L_s) = 1$$

$$\frac{g_m L_s}{(C_e + C_{gs})} = R_s$$

then,

$$i_1 = \frac{g_m \omega_0^2 L_s(C_e + C_{gs})}{R_s j\omega_0(C_e + C_{gs})} v_{gs}$$

$$= -j\omega_0(C_e + C_{gs}) v_{gs} \tag{D.35}$$

Then substituting Eq. (D.35) into Eq. (D.31), yields v_{gs}

$$v_{gs} = \left(-j\omega_0(C_e + C_{gs})v_{gs}\right) \cdot \frac{1}{j\omega_0(C_e + C_{gs})}$$

$$= -v_{gs} \qquad (D.36)$$

which means $v_{gs} = 0$.

Therefore,

$$\bar{\imath}_{n,o,R_{out}} = \bar{\imath}_{n,R_{out}} \qquad (D.37)$$

By observing the small-signal circuit in Figure D-4, no stimulation is present at the input circuit. which yields $i_1 = 0$ and $v_{gs} = 0$. Therefore, $\bar{\imath}_{n,o,R_{out}} = \bar{\imath}_{n,R_{out}}$.

Appendix E

Once the contributions of output noise due to the thermal noise sources are known, the noise factor is ready to be calculated. The four mean square currents due to thermal noise sources have been given in chapter three as follows,

$$\overline{\iota_{n,R_s}^2} = 4kT\frac{1}{R_s}\Delta f \tag{E.1}$$

$$\overline{\iota_{n,R_{out}}^2} = 4kT\frac{1}{R_{out}}\Delta f \tag{E.2}$$

$$\overline{\iota_{n,d}^2} = 4kT\gamma_{short}g_{d0}\Delta f \tag{E.3}$$

$$\overline{\iota_{n,g}^2} = 4kT\beta_{short}g_g\Delta f \tag{E.4}$$

As shown in previous section, the contributions of these four noise sources to the output noise current are

$$\bar{\iota}_{n,o,R_s} = \frac{g_m}{j2\omega_0 C_{tot}}\bar{\iota}_{n,R_s} \tag{E.5}$$

$$\bar{\iota}_{n,o,d} = -\frac{1}{2}\bar{\iota}_{n,d} \tag{E.6}$$

$$\bar{\iota}_{n,o,g} = \frac{g_m}{j\omega_0 C_{tot}}\frac{1 - jR_s\omega_0 C_{tot}}{j2R_s\omega_0 C_{tot}}\bar{\iota}_{n,g} \tag{E.7}$$

$$\bar{\iota}_{n,o,R_{out}} = \bar{\iota}_{n,R_{out}} \tag{E.8}$$

By definition, the noise factor can be expressed as

$$F = \frac{\overline{\iota^2}_{n,o,R_s} + \overline{\iota^2}_{n,o,d} + \overline{\iota^2}_{n,o,g} + \overline{\iota^2}_{n,o,correlation} + \overline{\iota^2}_{n,o,R_{out}}}{\overline{\iota^2}_{n,o,R_s}} \tag{E.9}$$

The output noise due to the correlation between channel thermal noise and induced gate noise can be represented as [18]

$$\overline{\iota^2}_{n,o,correlation} = \frac{g_m c}{2\omega_0 C_{tot}}\sqrt{\overline{\iota^2}_{n,g}\cdot\overline{\iota^2}_{n,d}} \tag{E.10}$$

where c is the correlation coefficient (see Appendix B).

Therefore, the noise factor can be calculated as

$$F = 1 + \frac{\left|-\frac{1}{2}\right|^2 \gamma_{short} g_{d0} + \left|\frac{g_m}{j\omega_0 C_{tot}} \frac{1-jR_s\omega_0 C_{tot}}{j2R_s\omega_0 C_{tot}}\right|^2 \beta_{short} g_g}{\left|\frac{g_m}{j2\omega_0 C_{tot}}\right|^2 \frac{1}{R_s}} +$$

$$\frac{\frac{g_m c}{2\omega_0 C_{tot}} \sqrt{\gamma_{short} g_{d0} \cdot \beta_{short} g_g} + \frac{1}{R_{out}}}{\left|\frac{g_m}{j2\omega_0 C_{tot}}\right|^2 \frac{1}{R_s}} \qquad (E.11)$$

where

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}}$$

Then after working through some algebra, the noise factor is formed to be,

$$F = 1 + \frac{\frac{1}{4}\gamma_{short} g_{d0} + \left(\frac{g_m}{\omega_0 C_{tot}}\right)^2 \frac{1+(R_s\omega_0 C_{tot})^2}{(2R_s\omega_0 C_{tot})^2} \beta_{short} \frac{{\omega_0}^2 C_{gs}^2}{5 g_{d0}}}{\left(\frac{g_m}{2\omega_0 C_{tot}}\right)^2 \frac{1}{R_s}} +$$

$$\frac{\frac{g_m c}{2\omega_0 C_{tot}} \sqrt{\gamma_{short} g_{d0} \cdot \beta_{short} \frac{{\omega_0}^2 C_{gs}^2}{5 g_{d0}}} + \frac{1}{R_{out}}}{\left(\frac{g_m}{2\omega_0 C_{tot}}\right)^2 \frac{1}{R_s}}$$

$$= 1 + \frac{\frac{1}{4}\gamma_{short} g_{d0} + g_m^2 \left(\frac{C_{gs}}{C_{tot}}\right)^2 \left(Q^2 + \frac{1}{4}\right) \beta_{short} \frac{1}{5 g_{d0}}}{g_m^2 R_s Q^2} +$$

$$\frac{\frac{C_{gs}}{C_{tot}} g_m c \sqrt{\frac{\gamma_{short} \cdot \beta_{short}}{20}} + \frac{1}{R_{out}}}{g_m^2 R_s Q^2} \qquad (E.12)$$

where the values of γ_{short}, β_{short} and c are extracted for short-channel devices.

Appendix F

In this appendix, analytical expressions for the output conductance and transconductance are discussed for both long-channel devices and short-channel devices.

F.1 Derivations of g_{d0} and g_m for Long-channel Devices

For long-channel devices, the well-known expressions of the drain current in both triode region and saturation region are given as [43]

$$I_{dtriode} = \mu_0 C_{ox} \frac{W}{L}\left(V_{od} \cdot V_{ds} - \frac{1}{2}V_{ds}^2\right) \quad (F.1)$$

$$I_{dsat} = \frac{1}{2}\mu_0 C_{ox} \frac{W}{L} V_{od}^2 \quad (F.2)$$

By definition, the output conductance g_d is

$$g_d = \frac{\partial I_{dtriode}}{\partial V_{ds}}\Big|_{V_{gs}}$$

$$= \mu_0 C_{ox} \frac{W}{L}\left(V_{od} - \frac{1}{2} \cdot 2\, V_{ds}\right)$$

$$= \mu_0 C_{ox} \frac{W}{L}(V_{od} - V_{ds}) \quad (F.3)$$

Therefore, the output conductance at zero bias (i.e. $V_{ds} = 0$), can be expressed by,

$$g_{d0} = g_d|_{V_{ds}=0}$$

$$= \mu_0 C_{ox} \frac{W}{L} V_{od}$$

$$= \mu_0 C_{ox} \frac{W}{L} \sqrt{2 I_{dsat} \frac{L}{W \mu_0 C_{ox}}}$$

$$= \sqrt{2 \frac{W}{L} \mu_0 C_{ox} I_{dsat}} \quad (F.4)$$

The transconductance of a long-channel device in saturation is given as,

$$g_m = \left.\frac{\partial I_{dsat}}{\partial V_{ds}}\right|_{V_{gs}}$$

$$= \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\cdot 2V_{od}$$

$$= \mu_0 C_{ox}\frac{W}{L}\cdot V_{od}$$

$$= \sqrt{2\frac{W}{L}\mu_0 C_{ox} I_{dsat}} \qquad (F.5)$$

For long-channel devices, it is obvious that the output conductance at zero bias g_{d0} has the same form as the transconductance in saturation in terms of V_{od} or I_{dsat}.

F.2 Derivations of g_{d0} and $g_m$for Short-channel Devices

However, the drain current for short-channel devices is expressed differently than for the long-channel devices. By taken some important short-channel effects into account, such as velocity saturation and channel-length modulation, the expressions of the analytical drain current model in both the triode region and saturation region are given by [11],

$$I_{dtriode} = \mu_{eff} C_{ox}\left(\frac{W}{L}\right)\cdot\frac{(V_{gs}-V_{th})V_{ds}-\left(\frac{m}{2}\right)V_{ds}^2}{1+(\mu_{eff}V_{ds})/(2v_{sat}L)} \qquad (F.6)$$

$$I_{dsat} = \mu_{eff} C_{ox}\left(\frac{W}{L}\right)\frac{\frac{(V_{gs}-V_{th})^2}{2m}}{1+\mu_{eff}(V_{gs}-V_{th})/(2mv_{sat}L)}\cdot(1+\lambda V_{ds}) \qquad (F.7)$$

where [11, 22],

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_{gs}-V_{th})} \qquad (F.8)$$

$$\theta = \frac{\beta_\theta}{t_{ox}} \tag{F.9}$$

$$m = 1 + \frac{\sqrt{\frac{\varepsilon_{si} q N_{ch}}{4\,\Psi_B}}}{C_{ox}} \tag{F.10}$$

$$\Psi_B = \left(\frac{kT}{q}\right)\ln(N_{ch}/n_i) \tag{F.11}$$

After applying the quotient rule, the output conductance g_d can be expressed as

$$g_d = \left.\frac{\partial I_{dtriode}}{\partial V_{ds}}\right|_{\mathrm{V_{gs}}}$$

$$= \mu_{eff} C_{ox}\left(\frac{W}{L}\right)\cdot \left[\frac{\left(V_{od}V_{ds} - \left(\frac{m}{2}\right)V_{ds}^2\right)'\cdot\left(1+\frac{\mu_{eff}V_{ds}}{2v_{sat}L}\right) - \left(V_{od}V_{ds} - \left(\frac{m}{2}\right)V_{ds}^2\right)\cdot\left(1+\frac{\mu_{eff}V_{ds}}{2v_{sat}L}\right)'}{\left(1+\frac{\mu_{eff}V_{ds}}{2v_{sat}L}\right)^2}\right]$$

$$= \mu_{eff} C_{ox}\left(\frac{W}{L}\right)\frac{(V_{od} - mV_{ds})\cdot\left(1+\frac{\mu_{eff}V_{ds}}{2v_{sat}L}\right) - \left(V_{od}V_{ds} - \left(\frac{m}{2}\right)V_{ds}^2\right)\cdot\frac{\mu_{eff}}{2v_{sat}L}}{\left(1+\frac{\mu_{eff}V_{ds}}{2v_{sat}L}\right)^2}$$

$$= \frac{\mu_{eff} C_{ox}\left(\frac{W}{L}\right)\left[V_{od} - mV_{ds} - \left(\frac{m}{2}\right)\frac{\mu_{eff}}{2v_{sat}L}V_{ds}^2\right]}{\left(1+\frac{\mu_{eff}V_{ds}}{2v_{sat}L}\right)^2} \tag{F.12}$$

Therefore, the output conductance at zero bias, which is $V_{ds} = 0$, can be expressed by,

$$g_{d0} = g_d|_{\mathrm{V_{ds}=0}} = \frac{\mu_0}{1+\theta V_{od}} C_{ox}\frac{W}{L}V_{od} \tag{F.13}$$

By substituting the effective mobility equation into the saturation drain current formula, the equation of I_{dsat} for short-channel devices can be rewritten as in following:

$$I_{dsat} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) \frac{\left(V_{gs} - V_{th}\right)^2/(2m)}{1 + \mu_{eff}\left(V_{gs} - V_{th}\right)/(2mv_{sat}L)} \cdot (1 + \lambda V_{ds}) \qquad (F.14)$$

The transconductance of a short-channel device in saturation is given as

$$g_m = \left.\frac{\partial I_{dsat}}{\partial V_{ds}}\right|_{\mathrm{V_{gs}}}$$

$$= \left[\frac{\mu_0}{1 + \theta V_{od}} C_{ox} \left(\frac{W}{L}\right) \frac{{V_{od}}^2/(2m)}{1 + \frac{\mu_0}{1+\theta V_{od}} \frac{1}{2mv_{sat}L} V_{od}} \cdot (1 + \lambda V_{ds})\right]'$$

$$= C_{ox}\mu_0 \left(\frac{W}{L}\right) \frac{1}{2m} (1 + \lambda V_{ds}) \cdot \left[\frac{{V_{od}}^2}{(1 + \theta V_{od})\left(1 + \frac{1}{2mv_{sat}L} \frac{\mu_0}{1+\theta V_{od}} V_{od}\right)}\right]'$$

$$= C_{ox}\mu_0 \left(\frac{W}{L}\right) \frac{1}{2m} (1 + \lambda V_{ds}) \cdot \left[\frac{{V_{od}}^2}{\left(1 + \theta V_{od} + \frac{\mu_0}{2mv_{sat}L} V_{od}\right)}\right]'$$

$$= C_{ox}\mu_0 \left(\frac{W}{L}\right) \frac{1}{2m} (1 + \lambda V_{ds})$$
$$\cdot \left[\frac{\left({V_{od}}^2\right)'\left(1 + \theta V_{od} + \frac{\mu_0}{2mv_{sat}L} V_{od}\right) - {V_{od}}^2\left(1 + \theta V_{od} + \frac{\mu_0}{2mv_{sat}L} V_{od}\right)'}{\left(1 + \theta V_{od} + \frac{\mu_0}{2mv_{sat}L} V_{od}\right)^2}\right]$$

$$= C_{ox}\mu_0 W v_{sat} \cdot (1 + \lambda\, V_{ds}) \cdot \frac{\left(4mv_{sat}LV_{od} + (2mv_{sat}L\theta + \mu_0){V_{od}}^2\right)}{(2mv_{sat}L + (2mv_{sat}L\theta + \mu_0)V_{od})^2} \qquad (F.15)$$

F.3 Calculations of Body Effect Factor m

In Eq. (F.10), the body effect factor m is given as [11]

$$m = 1 + \frac{\sqrt{\frac{\varepsilon_{si} q N_{ch}}{4\,\Psi_B}}}{C_{ox}}$$

where Ψ_B can be determined by

$$\Psi_B = \left(\frac{kT}{q}\right)\ln(N_{ch}/n_i)$$

The parameter N_{ch} is the channel doping concentration obtained from BSIM3 models in Appendix H. The parameter n_i is intrinsic carrier concentration, and its typical value is 1.5×10^{10} cm^{-3} for silicon at room temperature [39].

Therefore, the parameter values used in the calculation of m and the values of m are listed in Table F-1 for both 90 nm and 180 nm processes.

Table F-1: Parameters for calculation of the body effect factor m

Parameters	90 nm	180 nm
Oxide capacitance per unit area C_{ox}	0.014 F/m^2	0.00857 F/m^2
Channel doping concentration N_a	9.7×10^{17} cm^{-3}	2.3549×10^{17} cm^{-3}
Difference between Fermi potential and intrinsic potential Ψ_B	0.4658 V	0.429 V
Body effect coefficient m	1.21	1.18

Appendix G

G.1 MATLAB Script for Monomial Curve Fitting of the Transconductance g_m

```
%convert transconductance function to monomial format
%The following equation is used in this program
%output variable or dependent variable: gm
%design variables or independent variables: L, W, I_ds
%process constants: u_0,C_ox, v_sat,m,theta
%constraints: L_min,L_max,W_min,W_max, V_od_min,V_od_max,
%V_ds_min V_ds_max,
%gm=u_0*C_ox*W*v_sat*(2*V_od*2*m*v_sat*L+V_od^2*(2*m*v_sat*L*theta+u_0)
)/
%  (2*m*v_sat*L+V_od*(2*m*v_sat*L*theta+u_0))^2*(1+V_ds*Lamda)
%empirical function of monomial format
%gm=a0*(L^a1)*(W^a2)*(I_ds^a3);
%convert the aforementioned equation by taking log on both sides
%log_gm=log_a0+a1*log_L+a2*log_W+a3*log_I_ds

%set up process constants
u_0=1.7999999E-02; %m^2/VS
v_sat=1.1000000E+05; %m/s
m=1.20897;
theta=0.3; %1/V
C_ox=14.0538E-03; %F/m^2
Lamda=0.4

%set up dependent variables
L_min=0.09E-6;
L_max=0.45E-6;
W_min=1E-6;
W_max=100E-6;
V_od_min=0.1;
V_od_max=0.4;
Vds_min=0.5;
Vds_max=1;

N=30;
L=linspace(L_min,L_max,N)';
W=linspace(W_min,W_max,N)';
V_ds=linspace(Vds_min, Vds_max, N)';
V_od=linspace(V_od_min, V_od_max,N)';

%calculate gm
%initianize gm
gm=[];
I_ds=[];
design_var=[];
for(i=1:N)
    for(j=1:N)
        for (k=1:N)
        u_eff(k)=u_0/(1+theta*V_od(k));
        V_sat(k)=2*v_sat*L(i)/u_eff(k);
        V_dssat(k)=V_od(k)/m/(1+V_od(k)/(m*V_sat(k)));
        I_ds(k)=1/2*u_eff(k)*C_ox*W(j)/L(i)*V_od(k)*V_dssat(k)*...
```

```
        (1+Lamda*V_ds(k));
        I_ds=[I_ds; I_ds(k)];
        temp_gm=u_0*C_ox*W(j)*v_sat*(2*V_od(k)*2*m*v_sat*L(i)+ ...
               V_od(k)^2*(2*m*v_sat*L(i)*theta+u_0))/...
              (2*m*v_sat*L(i)+V_od(k)*(2*m*v_sat*L(i)*theta+u_0))^2*...
              (1+V_ds(k)*Lamda);
        gm = [gm; temp_gm];
        design_var=[design_var; [10 L(i) W(j) I_ds(k)]];
        end
    end
end

%log transformation
log_gm = log10(gm);
log_design_var = log10(design_var);

%multiple linear regression y=a0+a1*x1+a2*x2+a3*x3
y=log_gm;
X=log_design_var;
[b bint r rint stats] = regress(y,X);
a0=10^(b(1))
a1=b(2)
a2=b(3)
a3=b(4)

stats

%plot of error distribution
ybar=mean(y)
sserr=sum(r.*r)
sstot=sum((y-ybar).*(y-ybar))
%coefficient of determination (R-squared)
r2=1-sserr/sstot

residual=abs((r./y))*100;
subplot(2,1,1)
hist_ret=hist(residual, 100);
hist(residual, 100)
subplot(2,1,2)
cdfplot(abs(residual))
axis([0 10 0 1])
error_max=max(residual)
error_min=min(residual)
```

G.2 MATLAB Script for Monomial Curve Fitting of the Output Conductance g_{d0}

```
%convert output conductance function to monomial format
%The following equation is used in this program
%output variable or dependent variable: gd0
%design variables or independent variables: L, W, I_ds
%process constants: u_0,C_ox, v_sat,m,theta
%constraints: L_min,L_max,W_min,W_max, V_od_min,V_od_max,
%V_ds_min, V_ds_max
```

```
%gd0=u_eff*C_ox*W/L*V_od
%u_eff=u0/(1+Theta*V_od)
%Vdssat=V_od*Vsat/(V_od+m*Vsat)
%Vsat=2*vsat*L/u_eff
%empirical function of monomial format
%gdn=a0*(L^a1)*(W^a2)*(I_d^a3);
%convert the aforementioned equation by taking log on both sides
%log_gd0=log_a0+a1*log_L+a2*log_W+a3*log_I_ds

%set up process constants
u_0=1.7999999E-02; %m^2/VS
v_sat=1.1000000E+05; %m/s
m=1.20897;
theta=0.3; %1/V
C_ox=14.0538E-03; %F/m^2
Lamda=0.4;

%set up dependent variables
L_min=0.09E-6;
L_max=0.45E-6;
W_min=1E-6;
W_max=100E-6;
V_od_min=0.1;
V_od_max=0.4;
Vds_min=0.5;
Vds_max=1;

N=30;
V_ds=linspace(Vds_min, Vds_max, N)';
L=linspace(L_min,L_max,N)';
W=linspace(W_min,W_max,N)';
V_od=linspace(V_od_min, V_od_max,N)';

%calculate gd0
%initianize gd0
gd0=[];
I_ds=[];
design_var=[];
for(i=1:N)
    for (j=1:N)
        for (k=1:N)
            u_eff(k)=u_0/(1+theta*V_od(k));
            V_sat(k)=2*v_sat*L(i)/u_eff(k);
            V_dssat(k)=V_od(k)/m/(1+V_od(k)/(m*V_sat(k)));
            I_ds(k)=1/2*u_eff(k)*C_ox*W(j)/L(i)*V_od(k)*V_dssat(k)* ...
                    (1+Lamda*V_ds(k));
            temp_gd0=u_eff(k)*C_ox*W(j)/L(i)*V_od(k);
            gd0 = [gd0; temp_gd0];
            I_ds=[I_ds; I_ds(k)];
            design_var=[design_var; [10 L(i) W(j) I_ds(k)]];
        end
     end
end

%log transformation
log_gd0 = log10(gd0);
```

```
log_design_var = log10(design_var);

%multiple linear regression y=a0+a1*x1+a2*x2+a3*x3
y=log_gd0;
X=log_design_var;
[b bint r rint stats] = regress(y,X);
a0=10^(b(1))
a1=b(2)
a2=b(3)
a3=b(4)
stats

%plot of error distribution
ybar=mean(y)
sserr=sum(r.*r)
sstot=sum((y-ybar).*(y-ybar))
%coefficient of determination (R-squared)
r2=1-sserr/sstot

residual=abs((r./y))*100;
subplot(2,1,1)
hist(residual, 100)
hist_ret=hist(residual, 100);
subplot(2,1,2)
cdfplot(residual)
axis([0 10 0 1])
error_max=max(residual)
error_min=min(residual)
```

Appendix H

H.1 BSIM3 Model Card for 90 nm from Predictive Technology Model

*Predictive Technology Model Beta Version
* 90nm NMOS SPICE Parametersv (normal one)

```
.model CMOSN NMOS
+Level = 49
+Lint = 1.5e-08 Tox = 2.5e-09
+Vth0 = 0.2607 Rdsw = 180
+lmin=1.0e-7 lmax=1.0e-7 wmin=1.0e-7 wmax=1.0e-4
+Tref=27.0   version =3.1
+Xj= 4.0000000E-08       Nch= 9.7000000E+17
+lln= 1.0000000          lwn= 1.0000000              wln= 0.00
+wwn= 0.00               ll= 0.00
+lw= 0.00                lwl= 0.00                   wint= 0.00
+wl= 0.00                ww= 0.00                    wwl= 0.00
+Mobmod=  1              binunit= 2                  xl= 0.00
+xw= 0.00                binflag=  0
+Dwg= 0.00               Dwb= 0.00

+ACM= 0                  ldif=0.00                   hdif=0.00
+rsh= 7                  rd= 0                       rs= 0
+rsc= 0                  rdc= 0

+K1= 0.3950000           K2= 1.0000000E-02           K3= 0.00
+Dvt0= 1.0000000         Dvt1= 0.4000000             Dvt2= 0.1500000
+Dvt0w= 0.00             Dvt1w= 0.00                 Dvt2w= 0.00
+Nlx= 4.8000000E-08      W0= 0.00                    K3b= 0.00
+Ngate= 5.0000000E+20

+Vsat= 1.1000000E+05     Ua= -6.0000000E-10          Ub= 8.0000000E-19
+Uc= -2.9999999E-11
+Prwb= 0.00              Prwg= 0.00                  Wr= 1.0000000
+U0= 1.7999999E-02       A0= 1.1000000               Keta= 4.0000000E-02
+A1= 0.00                A2= 1.0000000               Ags= -1.0000000E-02
+B0= 0.00                B1= 0.00

+Voff= -2.9999999E-02    NFactor= 1.5000000          Cit= 0.00
+Cdsc= 0.00              Cdscb= 0.00                 Cdscd= 0.00
+Eta0= 0.1500000         Etab= 0.00                  Dsub= 0.6000000

+Pclm= 0.1000000         Pdiblc1= 1.2000000E-02      Pdiblc2= 7.5000000E-03
+Pdiblcb= -1.3500000E-02 Drout= 2.0000000            Pscbe1= 8.6600000E+08
+Pscbe2= 1.0000000E-20   Pvag= -0.2800000           Delta= 1.0000000E-02
+Alpha0= 0.00            Beta0= 30.0000000

+kt1= -0.3700000         kt2= -4.0000000E-02         At= 5.5000000E+04
+Ute= -1.4800000         Ua1= 9.5829000E-10          Ub1= -3.3473000E-19
+Uc1= 0.00               Kt1l= 4.0000000E-09         Prt= 0.00

+Cj= 0.0015              Mj= 0.72                    Pb= 1.25
```

```
+Cjsw= 2E-10          Mjsw= 0.37              Php= 0.773
+Cjgate= 2E-14        Cta= 0                  Ctp= 0
+Pta= 0               Ptp= 0                  JS=1.50E-08
+JSW=2.50E-13         N=1.0                   Xti=3.0
+Cgdo=3.493E-10       Cgso=3.493E-10          Cgbo=0.0E+00
+Capmod= 2            NQSMOD= 0               Elm= 5
+Xpart= 1             cgsl= 0.582E-10         cgdl= 0.582E-10
+ckappa= 0.28         cf= 1.177e-10           clc= 1.0000000E-07
+cle= 0.6000000       Dlc= 2E-08              Dwc= 0

*Predictive Technology Model Beta Version
*90nm PMOS SPICE Parametersv (normal one)

.model CMOSP PMOS
+Level = 49
+Lint = 1.5e-08 Tox = 2.5e-09
+Vth0 = -0.303 Rdsw = 300
+lmin=1.0e-7 lmax=1.0e-7 wmin=1.0e-7 wmax=1.0e-4
+Tref=27.0   version =3.1
+Xj= 4.0000000E-08          Nch= 1.0400000E+18
+lln= 1.0000000            lwn= 0.00               wln= 0.00
+wwn= 1.0000000            ll= 0.00                lw= 0.00
+lwl= 0.00                 wint= 0.00              wl= 0.00
+ww= 0.00                  wwl= 0.00               Mobmod=  1
+binunit= 2                xl= 0.00                xw= 0.00
+binflag=  0               Dwg= 0.00               Dwb= 0.00

+ACM= 0                   ldif=0.00               hdif=0.00
+rsh= 7                   rd= 0                   rs= 0
+rsc= 0                   rdc= 0

+K1= 0.3910000            K2= 1.0000000E-02        K3= 0.00
+Dvt0= 2.6700001          Dvt1= 0.5300000          Dvt2= 5.0000000E-02
+Dvt0w= 0.00              Dvt1w= 0.00              Dvt2w= 0.00
+Nlx= 7.5000000E-08       W0= 0.00                 K3b= 0.00
+Ngate= 5.0000000E+20

+Vsat= 1.0500000E+05      Ua= -5.0000000E-10       Ub= 1.5000000E-18
+Uc= -2.9999999E-11
+Prwb= 0.00               Prwg= 0.00               Wr= 1.0000000
+U0= 5.5000000E-03        A0= 2.0000000            Keta= 4.0000000E-02
+A1= 0.00                 A2= 0.9900000            Ags= -0.1000000
+B0= 0.00                 B1= 0.00

+Voff= -7.0000000E-02     NFactor= 1.5000000       Cit= 0.00
+Cdsc= 0.00               Cdscb= 0.00              Cdscd= 0.00
+Eta0= 0.2500000          Etab= 0.00               Dsub= 0.8000000

+Pclm= 0.1000000          Pdiblc1= 1.2000000E-02   Pdiblc2= 7.5000000E-03
+Pdiblcb= -1.3500000E-02  Drout= 0.9000000         Pscbe1= 8.6600000E+08
+Pscbe2= 1.0000000E-20    Pvag= -0.2800000         Delta= 1.0100000E-02
+Alpha0= 0.00             Beta0= 30.0000000

+kt1= -0.3400000          kt2= -5.2700000E-02      At= 0.00
```

```
+Ute= -1.2300000          Ua1= -8.6300000E-10          Ub1= 2.0000001E-18
+Uc1= 0.00               Kt1l= 4.0000000E-09          Prt= 0.00

+Cj= 0.0015              Mj= 0.7175511               Pb= 1.24859
+Cjsw= 2E-10             Mjsw= 0.3706993             Php= 0.7731149
+Cjgate= 2E-14           Cta= 9.290391E-04           Ctp= 7.456211E-04
+Pta= 1.527748E-03       Ptp= 1.56325E-03            JS=2.50E-08
+JSW=4.00E-13            N=1.0                      Xti=3.0
+Cgdo=3.49E-10           Cgso=3.49E-10               Cgbo=0.0E+00
+Capmod= 2               NQSMOD= 0                  Elm= 5
+Xpart= 1               cgsl= 0.582E-10             cgdl= 0.582E-10
+ckappa= 0.28            cf= 1.177e-10               clc= 5.4750000E-08
+cle= 6.4600000          Dlc= 2E-08                  Dwc= 0
```

H.2 BSIM3 Model Card for 180 nm from MOSIS

BSIM3 model card for 180 nm process from MOSIS
T16X SPICE BSIM3 VERSION 3.1 PARAMETERS

*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```
* DATE: Sep  7/01
* LOT: T16X                WAF: 1003
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                          LEVEL   = 8
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.3605538
+K1      = 0.5777152    K2      = 2.526592E-3 K3      = 2.670152E-3
+K3B     = 0.5204602    W0      = 1E-7        NLX     = 1.849791E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.5818674    DVT1    = 0.4236362   DVT2    = 0.0343793
+U0      = 288.0282273  UA      = -8.17815E-10  UB    = 1.450475E-18
+UC      = -8.34941E-12 VSAT    = 9.177422E4  A0      = 1.7971402
+AGS     = 0.345235     B0      = -8.186223E-9  B1    = -1E-7
+KETA    = 4.228174E-3  A1      = 2.883004E-4  A2     = 1
+RDSW    = 111.6421667  PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 0           LINT    = 1.013238E-8
+XL      = -2E-8        XW      = -1E-8       DWG     = -2.957794E-9
+DWB     = -5.481917E-9 VOFF    = -0.0751743  NFACTOR = 2.4279014
+CIT     = 0            CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.0617276   ETAB    = -0.0550759
+DSUB    = 0.9913143    PCLM    = 0.8440074   PDIBLC1 = 0.0740648
+PDIBLC2 = 0.01         PDIBLCB = -0.0967333  DROUT   = 0.5304348
+PSCBE1  = 7.990582E10  PSCBE2  = 2.575736E-8  PVAG    = 4.31952E-3
+DELTA   = 0.01         RSH     = 6.5         MOBMOD  = 1
+PRT     = 0            UTE     = -1.5        KT1     = -0.11
+KT1L    = 0            KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0            WLN     = 1           WW      = 0
+WWN     = 1            WWL     = 0           LL      = 0
+LLN     = 1            LW      = 0           LWN     = 1
+LWL     = 0            CAPMOD  = 2           XPART   = 0.5
+CGDO    = 7.27E-10     CGSO    = 7.27E-10    CGBO    = 1E-12
```

```
+CJ      = 9.84856E-4     PB      = 0.7346381      MJ      = 0.3585837
+CJSW    = 2.565078E-10   PBSW    = 0.5748835      MJSW    = 0.1326375
+CJSWG   = 3.3E-10        PBSWG   = 0.5748835      MJSWG   = 0.1326375
+CF      = 0              PVTH0   = 1.021475E-3    PRDSW   = -5
+PK2     = -1.325745E-3   WKETA   = 2.715841E-3    LKETA   = -9.467507E-3
+PU0     = 25.3593802     PUA     = 1.12333E-10    PUB     = 0
+PVSAT   = 1.773637E3     PETA0   = 1E-4           PKETA   = 2.106287E-3     )
*
.MODEL CMOSP PMOS (                               LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.4135147
+K1      = 0.5632651      K2      = 0.0362262      K3      = 0
+K3B     = 6.6196198      W0      = 1E-6           NLX     = 1.112495E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.4495656      DVT1    = 0.2548646      DVT2    = 0.1
+U0      = 117.9302546    UA      = 1.570536E-9    UB      = 1E-21
+UC      = -1E-10         VSAT    = 1.759454E5     A0      = 1.6471527
+AGS     = 0.3672404      B0      = 1.944686E-6    B1      = 4.821068E-6
+KETA    = 0.0195345      A1      = 0.0975486      A2      = 0.7207385
+RDSW    = 239.4418333    PRWG    = 0.5            PRWB    = -0.2029631
+WR      = 1              WINT    = 0              LINT    = 2.100806E-8
+XL      = -2E-8          XW      = -1E-8          DWG     = -2.681695E-8
+DWB     = 2.587904E-9    VOFF    = -0.0985781     NFACTOR = 2
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.2096608      ETAB    = -0.2204555
+DSUB    = 1.2864766      PCLM    = 2.5379236      PDIBLC1 = 6.306556E-3
+PDIBLC2 = 0.0507647      PDIBLCB = -1E-3          DROUT   = 9.98682E-4
+PSCBE1  = 1.732892E9     PSCBE2  = 5E-10          PVAG    = 14.9794054
+DELTA   = 0.01           RSH     = 7.2            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 6.96E-10       CGSO    = 6.96E-10       CGBO    = 1E-12
+CJ      = 1.20096E-3     PB      = 0.8591867      MJ      = 0.4126569
+CJSW    = 2.372671E-10   PBSW    = 0.7032518      MJSW    = 0.2835663
+CJSWG   = 4.22E-10       PBSWG   = 0.7032518      MJSWG   = 0.2835663
+CF      = 0              PVTH0   = 2.407623E-3    PRDSW   = 11.0156547
+PK2     = 3.195163E-3    WKETA   = 0.0269547      LKETA   = -4.288507E-3
+PU0     = -1.9784289     PUA     = -7.9036E-11    PUB     = 1E-21
+PVSAT   = -50            PETA0   = 1E-4           PKETA   = -2.470159E-3    )
```

Appendix I

In Eq. (F.9), a rough estimation for the vertical field degradation factor is given. The vertical field degradation factor θ and channel-length modulation are extracted from SPICE simulation IV curves. Examples are shown in Figure I-1 and I-2.

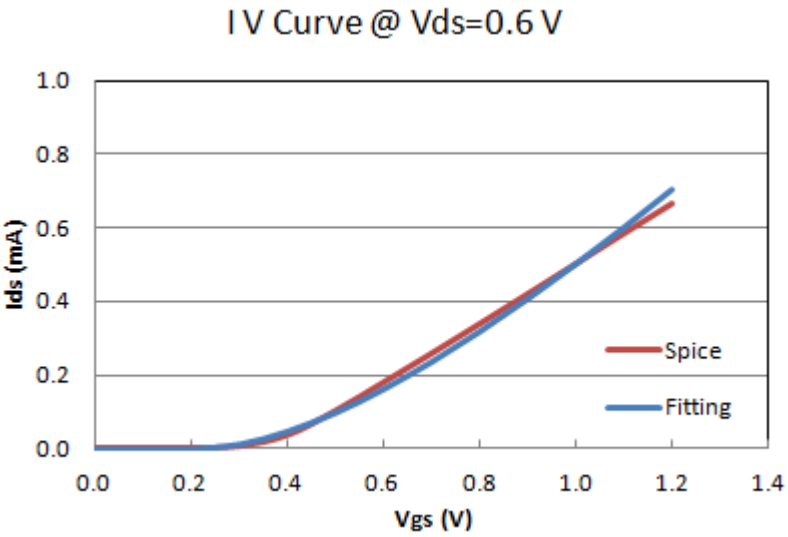


Figure I-1: Curve fitting for estimation of θ

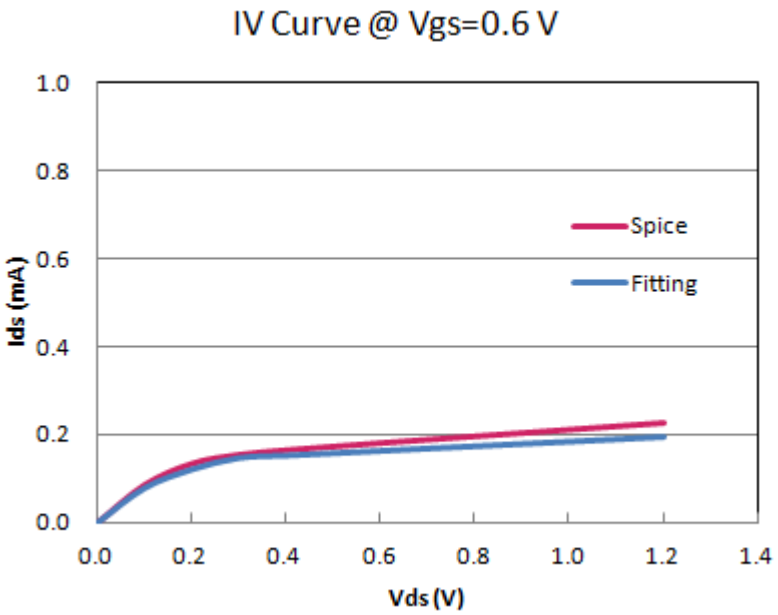
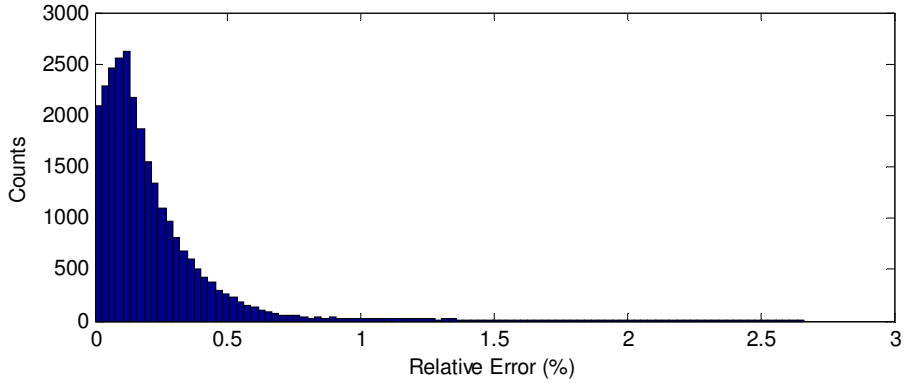


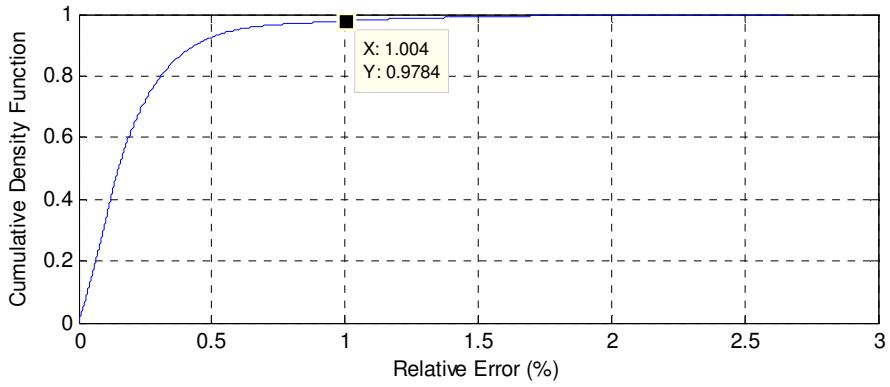
Figure I-2: Curve fitting for estimation of channel-length modulation parameter λ

Appendix J

The curve fitting results are shown in Figure J-1 and J-2 for 180 nm process. The coefficients of determination (R^2 value) for these two curve fittings are very close to 1 and more than 97% of curve fitting data have a relative error less than 1.0% for both cases.



(a)



(b)

Figure J-1: (a) Histogram of relative error for curve fitting of g_m for 180 nm, (b) Cumulative density function of relative error for curve fitting of g_m for 180 nm.

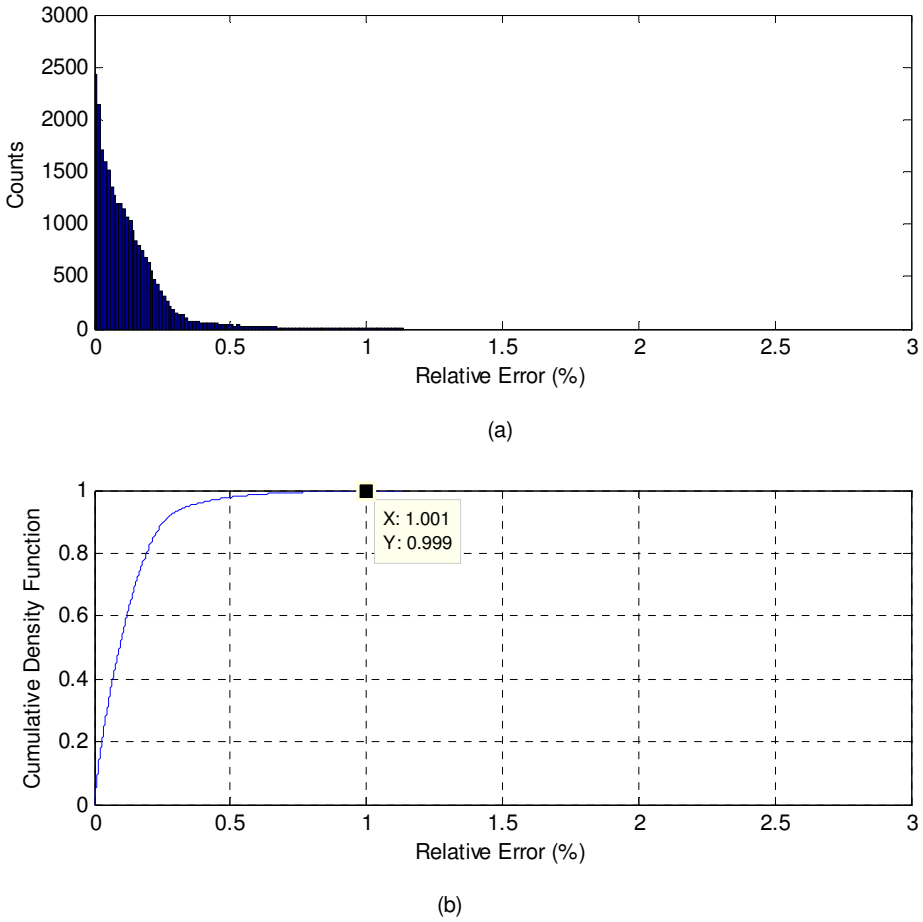


Figure J-2: (a) Histogram of relative error for curve fitting of g_{d0} for 180 nm, (b) Cumulative density function of relative error for curve fitting of g_{d0} for 180 nm.

Appendix K

MATLAB Script for GP Optimization

```
addpath h:\ut tyler\thesis\cvx
addpath h:\ut tyler\thesis\cvx\structures
addpath h:\ut tyler\thesis\cvx\lib
addpath h:\ut tyler\thesis\cvx\functions
addpath h:\ut tyler\thesis\cvx\commands
addpath h:\ut tyler\thesis\cvx\builtins

%%%% Optimized RF CMOS LNA Design Via Geometric Programming
%%%% 90 nm CMOS process
tic

Q_in=4;
Q_out=5;

%Thermal noise factor γ and β, coefficient c
GAMMA_sc=1.2;
BETA_sc=7.5;
c_sc=0.2;

%Process parameters
C_ox=14.0538*10^(-3);

%LNA parameters
R_s=50;
L_out=10*10^(-9)
f_0=2.4*10^9;
OMEGA_0=2*pi()*f_0;
R_out=Q_out*OMEGA_0*L_out
C_out=1/((2*pi()*f_0)^2*L_out)
L_min=0.09*10^(-6);
L_max=0.09*10^(-6);
W_min=1*10^(-6);
W_max=100*10^(-6);
C_t=1/(2*Q_in*OMEGA_0*R_s)
L_t=1/(OMEGA_0^2*C_t)
Vdd=2;

%Geometric programming
cvx_begin gp
    variables W L P C_gs L_s g_m g_d0 I_ds
    minimize
    1+(BETA_sc*(Q_in^2+1/4)*P^2*g_m^2/(5*g_d0)+GAMMA_sc/4*g_d0+...
    sqrt(GAMMA_sc*BETA_sc/20)*c_sc*P*g_m+1/R_out)/(R_s*Q_in^2*g_m^2);

    subject to
```

```
            L>=L_min;
            L<=L_max;
            W>=W_min;
            W<=W_max;
            P==C_gs/C_t;
            P<=1;
            3/2*C_gs*C_ox^(-1)*W^(-1)*L^(-1)==1;
            0.02*(g_m/C_t)*L_s==1;
            I_ds*Vdd<=0.001;
            g_m==0.0423*L^(-0.4578)*W^(0.5275)*I_ds^0.4725;
            g_d0==0.0091*L^(-0.5637)*W^(0.5305)*I_ds^0.4695;
cvx_end
F=1+(BETA_sc*(Q_in^2+1/4)*P^2*g_m^2/(5*g_d0)+GAMMA_sc/4*g_d0+...
      sqrt(GAMMA_sc*BETA_sc/20)*c_sc*P*g_m+1/R_out)/(R_s*Q_in^2*g_m^2);
g_d0opt=g_d0
g_mopt=g_m
Wopt=W
Lopt=L
Popt=P
C_gs_opt=C_gs
C_d_opt=C_t-C_gs_opt
L_s_opt=L_s
L_g_opt=L_t-L_s_opt
Ids_opt=I_ds
Fmin=10*log10(F)

toc
```

Appendix L

Same trade-off curves have been plotted for 180 nm LNA design and listed in this appendix.

L.1 Effect of Input Circuit Quality Factor on the Design of LNAs

For example, when the gate width equals 20 μm and channel length is 180 nm, a series of tradeoff curves have been plotted, which has confirmed that there is an optimal value for input circuit quality factor, the optimal quality factors display a small increase and the range is from 4 to 6 as shown in Figure L-1 for 180 nm design.

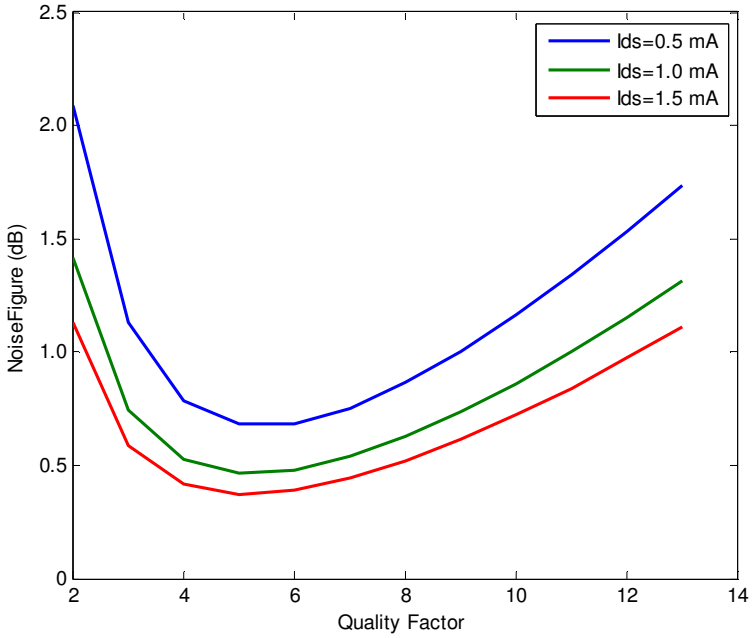


Figure L-1: Effect of input circuit quality factor on the noise figure at different dc drain current (W=20 μm, L=180 nm)

L.2 Effect of Input Circuit Quality Factor on the Noise Figure and Gate Width

Tradeoff analyses have also shown the influence of input circuit quality factor on the relationship of the obtained noise figure and the gate width (Figure L-2).

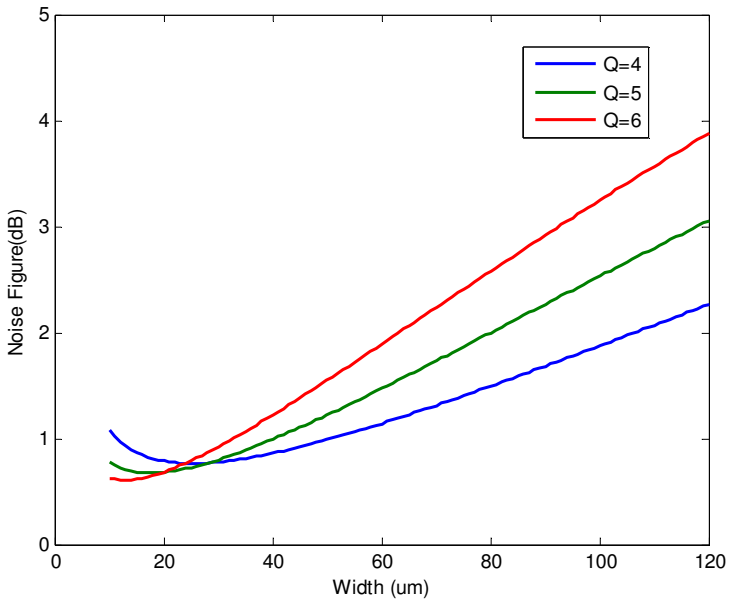


Figure L-2: Effect of channel width on the noise figure at different input circuit quality factors

Furthermore, such results can be visualized with 3-D plots in Figure L-3. Minimum noise figure can be achieved when either input circuit quality factor or channel width is fixed.

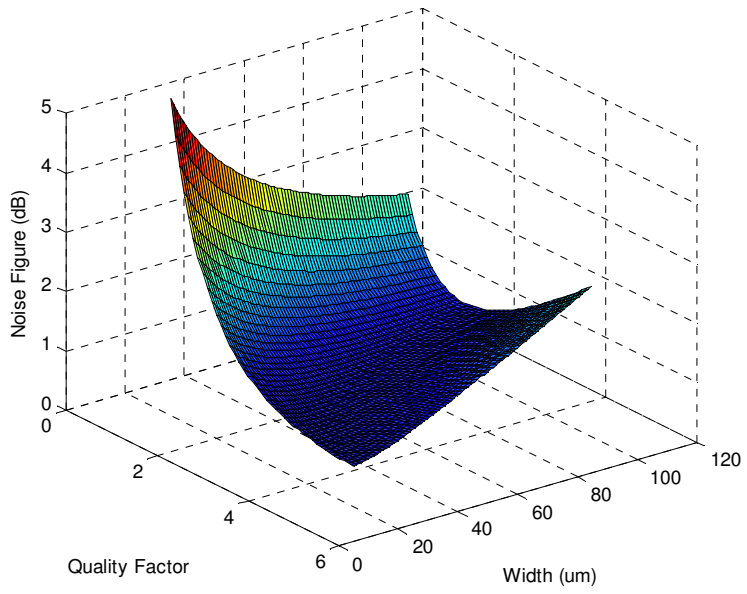


Figure L-3: Effect of input circuit quality factor and channel width on the noise figure in 3D

L.3 Effect of Drain Current and Operational Frequency on the Noise Figure

Drain current appears to have great influence on noise figure when the drain current is at a smaller scale less than 1 mA (Figure L-4). However, there is not much variation of noise figure when the drain current changes from 1 mA to 4 mA. Such results can also be easily visualized from 3D plot (Figure L-5).

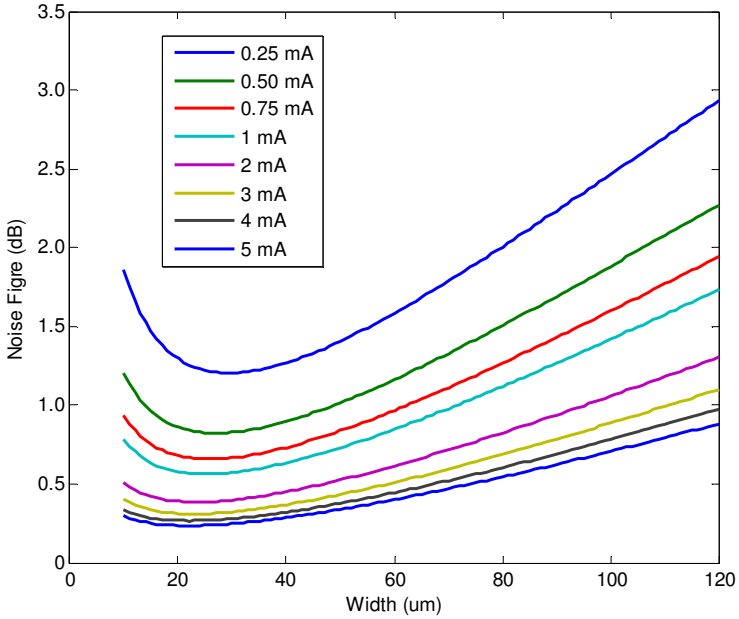


Figure L-4: Effect of channel width on the noise figure at different drain currents

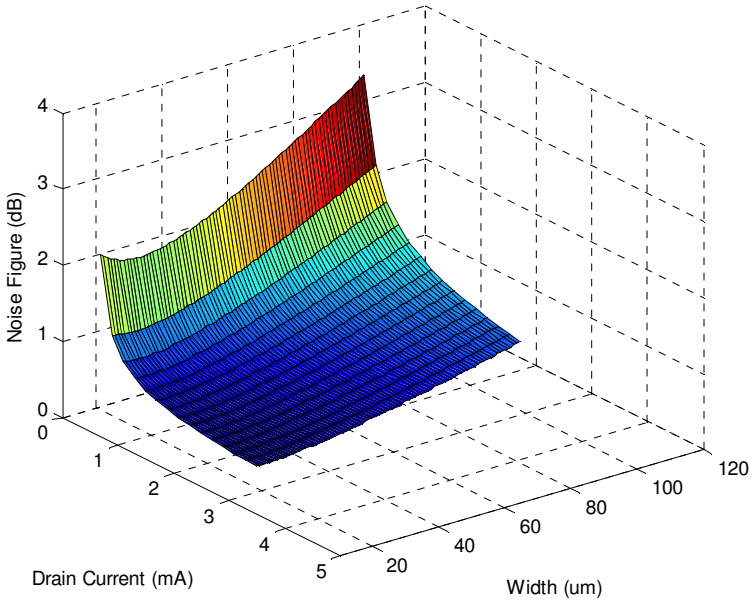


Figure L-5: Effect of drain current and channel width on the noise figure in 3D

Variation of operational frequency has great influence on the noise figure (Figure L-6 and L-7). However, our study focuses on narrowband application. The operating frequency is fixed at 2.4 GHz. Therefore, the influence of operational frequency on the noise figure is limited.

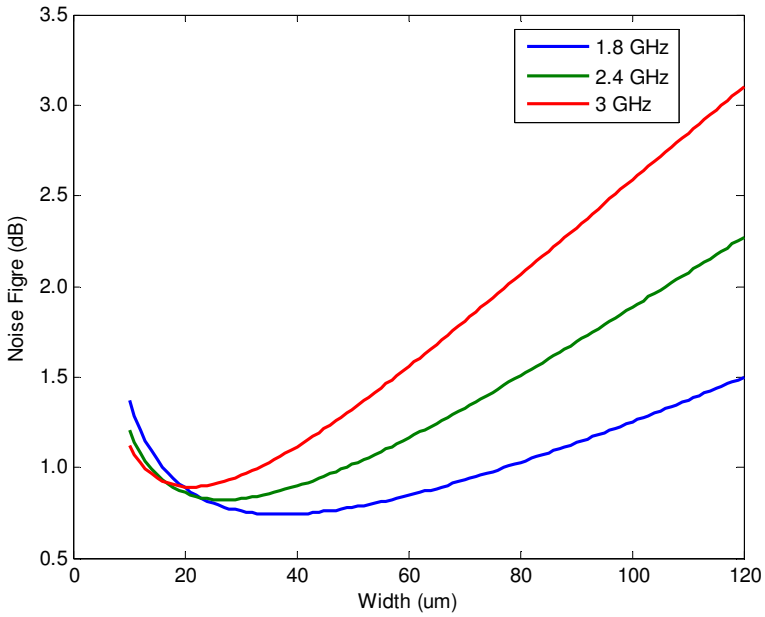


Figure L-6: Effect of channel width on the noise figure at different frequencies

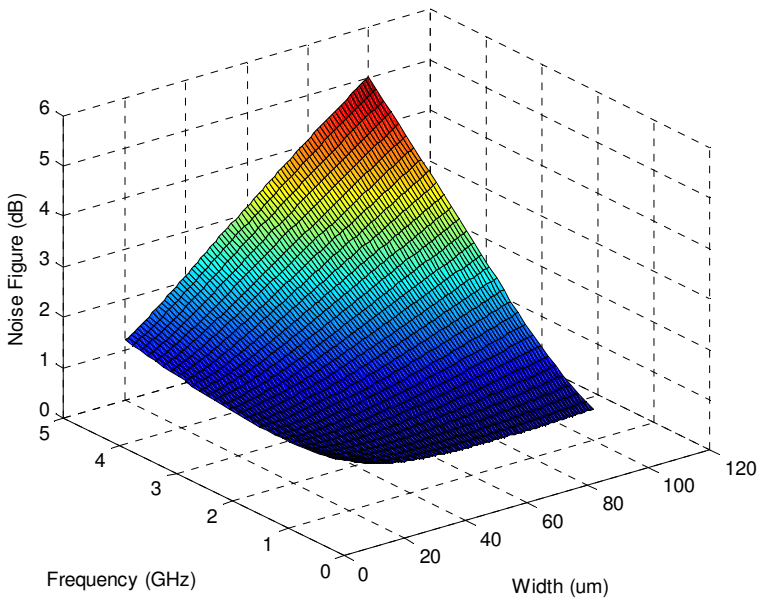


Figure L-7: Effect of operational frequency and channel width on the noise figure in 3D